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A 6-bit absolute value detector based on MOSFET and PTL structure

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Abstract. As science and technology develop fast, people nowadays can have an easy approach to various advanced products. The use of Internet of Things has become a reality. To ensure its reliable implementation in daily life, stable and efficient hardware equipment like sensor is essential, where absolute value detector is widely used. A detector is created on the basis of this. The circuit can compare a signed 6-bit number with the threshold of a 5-bit number. This design uses MOS and pass-transistor logic (PLT) structure as the basic parts to form the transcoding logic and the subtraction logic. This paper also discusses the optimization of its minimum latency and energy usage based on logic effort parameters. In order to match a sequence of minimum delays, the article gives various power supply voltages and calculates each scheme's lowest energy consumption for each voltage. The reduction of the energy cost is significant, which means the circuit has application value in reality. Besides, the different results are listed in a scatterplot to find out the trend of optimization, which may be helpful for selecting a proper scheme in the real program.

Keywords: Absolute Value Detector, Delay, Energy Consumption, Optimization, Logic Effort.

1. Introduction

Science and technology advancements have progressively introduced ideas like the Internet of Things into people's daily lives, drastically altering our lives [1]. Among them, the application of various sensors provides a great guarantee for intelligent life. The absolute value detector is an important part of different sensors. Detector helps extract useful information from complex signals for control, monitoring, diagnosis, and processing of various real-world situations [2-4]. For example, it can realize the rectification of the waveform [5]. And then it can be applied to the simplified analysis of image signals [6].

In this paper, the design and optimization of a MOS and PTL-based 6-bit absolute value detector are realized. The detector can compare a signed 6-bit number with a positive 5-bit input threshold. In the design part, the paper discusses the logical topology structure, and tries to implement specific circuits in a more efficient way. Then considering the size and supply voltage of each stage, we discuss the optimization of delay and energy consumption based on logical effort. Firstly, according to some basic assumptions of the paper, the specific parameters of each type of logic gate are given. Then, based on the critical path, the benchmark for optimization can be calculated. After obtaining the benchmark, the paper uses the Solver Adder-in in Excel to carry out the overall optimization. Also, we change the upper limit of the delay, and obtain multiple sets of optimization schemes to draw a scatter diagram, which

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may provide some regular suggestions for similar optimization. In all, energy consumption can decrease by more than 60% at over 1.3 times of minimum delay.

2. Topology of total design

2.1. Basic logic of the whole circuit

In this 6-bit binary absolute value detector, it is allowed to input a non-zero 6-bit 2's complement (including a sign bit) as the number to be compared and a 5-bit positive value (excluding the sign bit) as the threshold. The circuit will compare the absolute value of the 2's complement with the threshold. Finally, if the output value is 1, the absolute value of the input 6-bit two's complement is less than or equal to the input threshold. In this design, the paper aims to use an adder to subtract the two inputs, and the comparison result will be obtained by determining the sign of the difference after the operation.

2.2. Transcoding logic for processing the input signals

In the first transcoding part, the paper will use the absolute value of the six-bit two's complement as the subtrahend. The paper categorizes the actual input scenarios for discussion. Specifically, it will be divided into two parts: if the input is negative, no conversion is needed, and it can be directly used as a subtrahend with a minus sign through the second part adder for calculation; if the input is positive, it needs to be converted into the two's complement of its negative value for calculation. According to the rules of two's complement arithmetic, the following expression can be obtained:

$$X_6X_5X_4X_3X_2X_1 = \overline{A}_6\overline{A}_5\overline{A}_4\overline{A}_3\overline{A}_2\overline{A}_1 + 1 \quad (1)$$

Where X_{6-1} is the processed subtrahend and A_{6-1} is the input of six-bit signed number. In the circuit, the last term of the formula can be used as the carry-in of the first-level adder in the second part.

Therefore, in the first part, it is only necessary to perform a conversion on positive inputs. This design utilizes a pass-transistor logic (PTL) to implement the multiplexer (MUX) function, thereby achieving the above function. The specific circuit structure is illustrated in Figure 1.

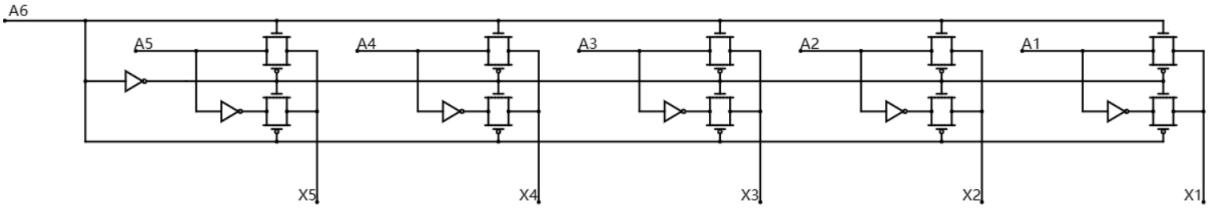

Figure 1. The structure of MUX (Photo/Picture credit: Original).

As the sign bit, the value of A_6 determines whether the input section needs to undergo a conversion. The function of the MUX is also based on this [7].

2.3. Subtraction logic for comparing

In the second part, the design aims to implement the functionality of an adder to compare the threshold with the input value. Upon analysis, it's observed that the adder in this circuit always performs the addition of a positive number and a negative number. However, for comparison, it's only necessary to focus on the carry-out of the last stage. Furthermore, because the last stage of the adder always involves the addition of 0 and 1, only the carry-out from the fifth stage of the adder is needed to reflect the final comparison outcome. Therefore, in this design, there will be five stages of adders involved in the operation.

For the structure of the adder, since this design only requires the carry-out from each stage, it can be simplified to some extent [8]. Assuming the threshold input is B, the actual required output is the carry-

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out of the highest bit of the sum of $X_5X_4X_3X_2X_1 + B_5B_4B_3B_2B_1$. To achieve a shorter delay time, the paper employs a parallel structure for computation, based on the half-adder structure:

$$P_i = X_i \oplus B_i \tag{2}$$

$$G_i = X_i B_i \tag{3}$$

P_i and G_i in expressions means propagate status and generate status of every bit respectively, and i refers to the different bit ranging from 1 to 5. To get the P_i and G_i, the precise circuit is displayed in Figure 2.

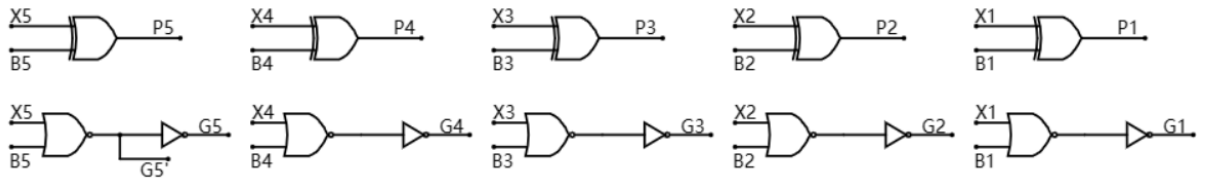

Figure 2. The structures of P_{1-5} and G_{1-5} generators (Photo/Picture credit: Original).

As shown in figure 2, X_{5-1}, G_{5-1} and $G_5{}'$ can be generated. The carry-outs for each stage can be expressed as follows:

$$C_i = P_i C_{i-1} + G_i \tag{4}$$

C_i represents the carry of the i-th bit. Substitute them into X_{5-1} and B_{6-1} respectively to get the following expression, where F refers to the output:

$$F = P_5P_4P_3P_2P_1C_0 + P_5P_4P_3P_2G_1 + P_5P_4P_3G_2 + P_5P_4G_3 + P_5G_4 + G_5 \tag{5}$$

This design uses a chain to realize the expression of logic from P_5 to $P_5P_4P_3P_2P_1$, as shown in Figure 3.

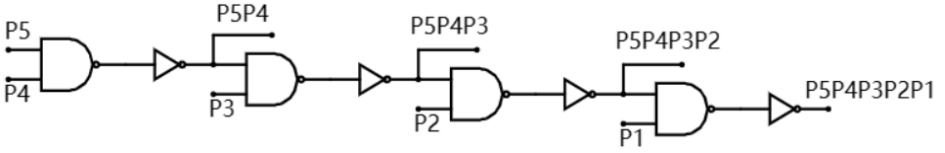

Figure 3. The logic chain to obtain the logic expression from P_5 to $P_5P_4P_3P_2P_1$ (Photo/Picture credit: Original).

Additionally, the design employs inverters, NAND gates, and NOR gates to produce the desired final output logic shown in Figure 4. Figures 2 and 3 contain data for each input on the left.

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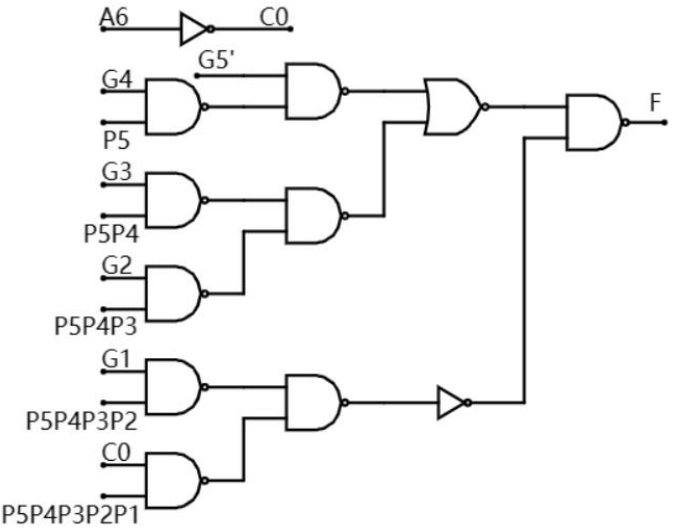

Figure 4. The other part to calculate the final output (Photo/Picture credit: Original).

3. Optimization of the delay and energy consumption

3.1. Parameters and structure of the single gate

Before proceeding with size and voltage optimization, the fundamental structure of gates and their corresponding parameters must be defined. In the calculations and optimizations, this paper makes the following assumptions: i) The unit-sized inverter is used to simplify the calculation, whose parameters are W_p=650nm, W_n= 430nm, $V_T = 0.2V$, L_p=L_n=100nm, γ ($C_{parasitic}$/ C_{gate}) = 1. ii) All inputs have input capacitances that are less than or equal to two inverters of the same size. iii) The C_L=32 unit-sized inverters are loaded into the output bit. iv) The power supply voltage (V_{DD}) is ranging at 0-1V.

The paper utilizes MUX, NAND gates, NOR gates, inverters, and XOR gates to implement all functions. Among these, MUX and XOR gates both employ the PTL structure, as illustrated in the Figure 5.

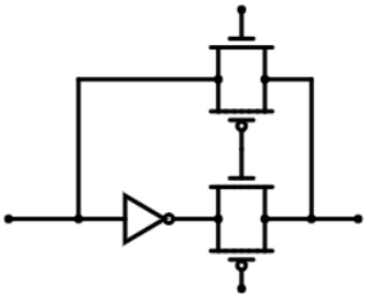

Figure 5. The structure of the PTL (Photo/Picture credit: Original).

When calculating parameters, the inverter and PTL gate can be treated as a compound gate, according to Figure 6.

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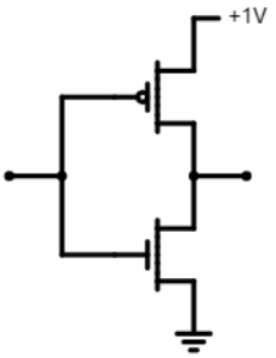
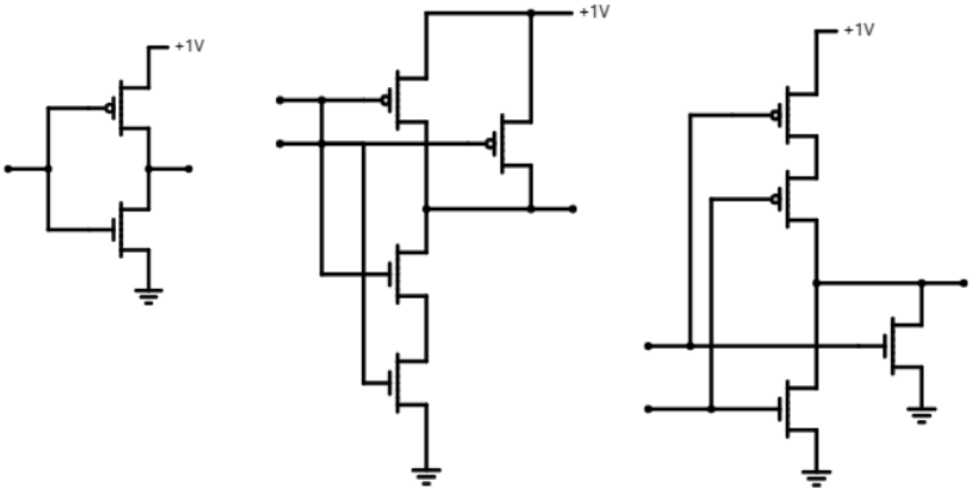


Figure 6. The structure of the compound gate (Photo/Picture credit: Original).

The rest of the structures are as Figure 7.



(a) (b) (c)

Figure 7. (a) The structure of the inverter; (b) The structure of the NOR gate; (c) The structure of the NAND gate (Photo/Picture credit: Original).

After calculation, the optimization below is mainly based on the parameters that are displayed in Table 1.

Table 1. The parameters of different gates used in this paper.

Gate type	g	p
Inverter	1	1
NAND	1.398	2
NOR	1.602	2
Compound Gate	2	3.185

3.2. Benchmark for optimization

Not only should the circuit's functionality be considered when designing digital circuits, but also the latency and energy usage. The critical path can help designers better analyze this problem. The critical path is the longest in the circuit, which affects the logic delay and performance of the entire system. In this part, the paper will analyze the specific delay and energy consumption on the critical path, and use it as a benchmark for the entire subsequent optimization.

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The critical path of this circuit contains a total of 15 stages (including an inverter as the initial drive), including 6 inverters, 2 PTL gates, 7 NAND gates, and 4 branch structures. The precise route is displayed in Figure 8 [9].

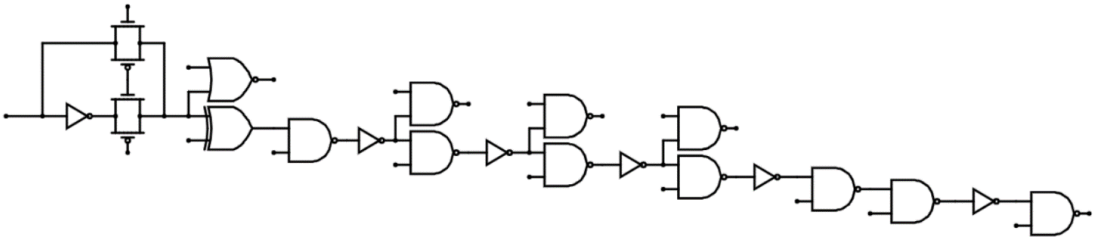

Figure 8. The critical path of the design (Photo/Picture credit: Original).

The minimum delay can be calculated by the following formulas:

Path Logical Effort: $$G = 1^6 \times 2^2 \times 1.398^7 \quad (6)$$

Path Branch Effect: $$B = \frac{2+1.602}{2} \times 2 \times 2 \quad (7)$$

Path Electrical Fanout: $$H = 32 \quad (8)$$

Path Effort: $$F = G \cdot B \cdot H = 9623.518 \quad (9)$$

Stage Effort: $$f^* = \sqrt[15]{F} = 1.843 \quad (10)$$

Total Path Delay: $$D_{min} = f^* \cdot N + \sum P = 1.843 \times 15 + 1 \times 6 + 3.185 \times 2 + 2 \times 7 = 54.015 \quad (11)$$

N refer to the number of the stages in critical path.

Also, to calculate the energy consumption, the expression below is necessary:

Path Effort: $$f_i = g_i \cdot h_i \quad (12)$$

Fanout: $$h = \frac{C_{out}}{C_{in}} \quad (13)$$

C_{out} and C_{in} are the input and output capacitance of every stage respectively, and f_i, g_i and h_i are the parameters of every gate. Table 2 displays each gate's size.

Table 2. The parameters and size of every gate on critical path.

Stage	Gate	g	p	b	size
1	INV	1	1	1	1
2	TG	2	3.185	1	3.657
3	TG	2	3.185	1.801	3.369
4	NAND	1.398	2	1	1.724
5	INV	1	1	1	2.272
6	NAND	1.398	2	2	4.189
7	INV	1	1	1	2.761
8	NAND	1.398	2	2	5.089
9	INV	1	1	1	3.354
10	NAND	1.398	2	2	6.182
11	INV	1	1	1	4.075
12	NAND	1.398	2	1	7.51
13	NAND	1.398	2	1	9.99
14	INV	1	1	1	13.17
15	NAND	1.398	2	1	24.273

When V_{DD} =1V,$E_{max} = 124.615$.So far, the optimized benchmark has been calculated through the critical path, the minimum delay time is 54.015, and if V_{DD}=1V, the energy consumption is 124.615.

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3.3. Size and power scaling

The size of the gate is directly related to the circuit capacitance. Changing the size means changing the total capacitance, which also means changing the delay and power consumption. At the same time, the power supply voltage will also affect the system delay and energy consumption. Therefore, how to balance the size and voltage, delay and power consumption will be the key points in the optimization part.

This paper uses Excel Solver Add-in as an optimization tool. For the specific setting, by setting the size of each gate and V_{DD} as variable numbers, the maximum delay is constrained to obtain the minimum energy consumption. The calculation formulas of relevant variables are listed below:

Parameters of Power Supply Voltage: $$K = \frac{(0.8)^2 V_{DD}}{(V_{DD}-V_T)^2} \quad (14)$$

Delay of every gate: $$D_i = g_i \cdot h_i + p_i \quad (15)$$

Delay of all: $$D_{tot} = K \cdot \sum Di \quad (16)$$

Minimum energy consumption: $$E_{min} = C \cdot V_{DD}^2 \quad (17)$$

During the calculation, by gradually changing the upper limit of the delay, there are different kinds of optimization schemes. For example, when the 1.5x delay is used as the constraint condition, Table 3 can be obtained through Solver Add-in.

Table 3. Size of every gate on critical path considering the size scaling and Power Supply Voltage.

Stage	Gate	Size	Energy	Delay
1	INV	1.081	1.081	1.974
2	TG	1.053	1.053	5.106
3	TG	1.011	1.822	6.746
4	NAND	1	1	3.398
5	INV	1	1	2
6	NAND	1	2	4.796
7	INV	1	1	2
8	NAND	1	2	4.796
9	INV	1	1	2.000
10	NAND	1	2	4.796
11	INV	1	1	2
12	NAND	1	1	3.398
13	NAND	1	1	4.134
14	INV	1.527	1.527	4.513
15	NAND	5.363	5.363	10.342
16	Load	32	32	32

Under the limitation of 1.5x delay, the energy consumption is 39.615, which is 68.21% lower than that at the beginning, and V_{DD} is 0.842V at this time. In the same way, by gradually changing the delay limit, a series of optimization schemes can be obtained, as shown in Table 4.

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Table 4. The energy reduction with varied delay limits.

Delay	VDD	Energy	Energy Reduction
54.015 (1.0x)	1V	124.615	
70.219 (1.3x)	0.919V	47.434	61.94%
75.621 (1.4x)	0.877V	43.169	65.36%
81.023 (1.5x)	0.842V	39.615	68.21%
86.424 (1.6x)	0.810V	36.615	70.62%
91.826 (1.7x)	0.781V	34.054	72.67%

By drawing the data of the benchmark and the optimized data from 1.3x delay to 1.7x delay on the scatter diagram, the image shown in Figure 9 can be obtained, from which some rules can be further analyzed.

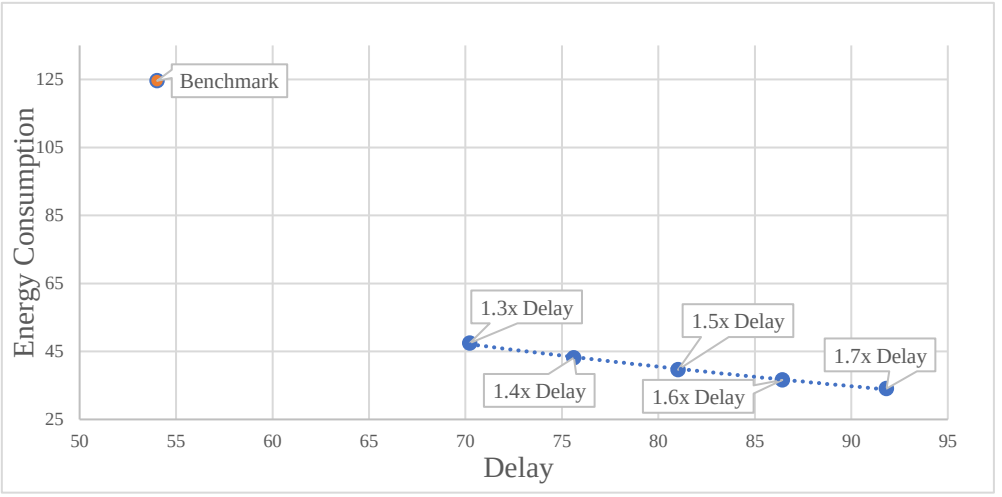

Figure 9. The relationships of delay and energy after the optimization (Photo/Picture credit: Original).

From Figure 9, it can be easily seen that for this circuit, problems with delay and energy consumption are always trade-off issues. Compared with the benchmark, by optimizing the scaling and power supply voltage, the original energy consumption is reduced by more than 60%, but correspondingly, lower energy consumption requires a larger delay. Therefore, when the delay limit increases to a certain extent, continuing to increase the delay is not very effective in reducing energy consumption. What's more, the trade-off between these two parameters needs to be selected in combination with actual conditions, such as technology, product demand, price, and other factors [10].

4. Conclusions

In this paper, a parallel structure is used to construct a 6-bit absolute value detector with a minimal delay. At the same time, by optimizing the size scaling and power supply voltage, we have obtained different optimization schemes under different delay constraints. The energy consumption drops by about 61.94% at the limit of 1.3 times of delay, and when the delay reaches 1.7 times, the energy consumption is reduced by 72.67%. From the scatter diagram (Figure 9), it can be analyzed that a shorter delay always contradicts a smaller energy consumption, and when the delay limit increases to a certain extent, the minimum energy consumption obtained by adjusting the power supply voltage and scaling is not cost-effective enough, so it may be necessary to seek other aspects for further optimization and analysis. In addition, there are many areas that can be optimized that are not covered in this paper. In this design, we have adopted many parallel topologies to realize the functions, but in fact, such a parallel structure will lead to an increase in the demand for the area of the circuit, which is not suitable for manufacturing

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and cost control. And the selection of semiconductor materials is also a direction worthy of discussion in future research.

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