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A methodology of designing and optimising a 4-bit absolute-value detector for the application of Brain-computer Interface

Yixiao Zhou

School of Electrical and Electronic Engineering, Nanyang Technological University, 639798, Singapore

yzhou055@e.ntu.edu.sg

Abstract. Digital integrated circuits perform logical operations through several modules composed of logic gates. As a common module in digital circuits, the absolute value detector is applied to compare the absolute value of two binary inputs and can be further used for data sorting and searching. In clinical medicine, the detector can receive biological data from the sensor and control the instrument on the operating table. A typical application is Brain-computer Interface (BCI). Therefore, the performance of detectors is significant to electronic devices like computers. The optimisation of detectors usually concentrates on their propagation delay and power consumption. But theoretical optimisation will inevitably use simple logic and have large fan-in, and it is difficult to be implemented in practice. Here we explore an alternative plan that is more convenient to be produced in the industry, which combines static complementary metal-oxide semiconductor (CMOS) technology and transmission gates. After gate sizing, the critical path calculates the propagation delay and energy based on the logical effort theory. Finally, the relationship between energy and delay is analysed by scaling the voltage supply and the minimum energy occurs when the delay grows to 1.5 times the minimum delay.

Keywords: Absolute-value Detector, Brain-computer Interface, CMOS, Digital Integrated Circuits.

1. Introduction

In recent years, wearable sensors have been widely used. A typical device is a smartwatch. It can detect health data such as blood oxygen levels and heart rate through photoelectric sensors in it. In fact, many human physiological activities contain detectable electrical and magnetic signals. For instance, a professional doctor can determine a diagnosis based on the electrical activity of the heart through an electrocardiogram (ECG), while an electroencephalogram (EEG) is capable of recording the electrical signals of the brain with electrodes that are attached to the scalp. As an organ connected to the spinal cord, the brain is responsible for controlling almost every physiological function. Since EEG was first used to record the electrical activity of the brain in 1924, great progress has been made in this field. In the 1970s, the University of California, Los Angeles, began research on neuro-prosthetics, which also gave birth to the concept of Brain-Computer Interface [1]. BCIs are computer-based systems that allow communications between the brain and the machine and can analyse the brain's signals or use them as feedback for instruments. The target population for this technology is usually medical patients who have

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severe motor dysfunction or cognitive impairments, such as locked-in syndrome (LiS) and Parkinson's disease (PD) [2].

In this paper, the absolute-value detector (AVD) used to detect signals in BCIs will be discussed, including the design and optimisation. The design of the circuit will provide an academic justification of the topology and logic gate implementation, and optimisations will focus on the balance of energy and delay. The size of transistors and power supply voltage will be considered as two variables for the optimisation process. For the purpose of clarifying the importance of AVD in this field, it is necessary to explain the operating principle and application background of BCIs.

2. Principles of BCIs

Similar to the working principle of most feedback systems, the operation mode of BCIs also require going through the basic steps of signal input, signal processing and signal output, as shown in figure 1. Obviously, the input signal here is the electrical or magnetic signal produced by the brain. In the signal processing part, these recorded signals need to be filtered, identified, and classified to generate the correct instructions to provide to the BCI device. In the modern healthcare system, devices for measuring brain signals are largely non-invasive. These devices consist of sensors placed on the scalp that measure the potential of an EEG or magnetoencephalography (MEG). Invasive devices are applied only in extreme cases and cannot avoid the risks of rejection reactions and neurosurgery itself. Therefore, semi-invasive devices that do not need to penetrate the cerebral cortex have been developed to reduce these risks. The typical signal that these devices can measure is the electrocorticography (ECoG). At present, BCIs still have limitations in the accuracy of signal acquisition. On the one hand, signals received by the sensor of a non-invasive device have passed a long distance and noise will inevitably mix in. On the other hand, due to the restriction of the number of electrodes, errors in sampled signals are possible for invasive techniques [3, 4]. If BCIs are to be applied more widely in healthcare, electromagnetic compatibility between electronic devices are also required to be considered, since there will be more than one device in the hospital room.

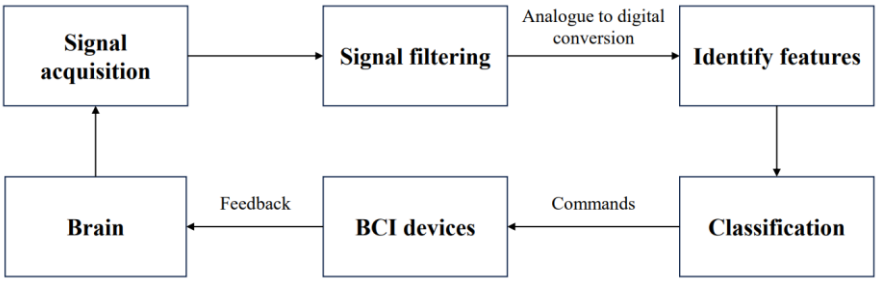

Figure 1. Operations of BCIs (Photo/Picture credit: Original).

In order to accurately detect signals from the brain, spike-sorting is developed in chips for neural engineering [5]. It can record the spike of a large number of neurons simultaneously and separate the data of a single neuron to achieve classification function. In terms of hardware implementation, an AVD is one of the most suitable circuits for spike detection. AVDs can receive an input signal, usually in the form of 2's complement, and then compare it to a threshold value. Therefore, an AVD consists of two portions: the transcoder and the comparator. The transcoder aims to extract the magnitude of the input while the comparator is used to make the comparison. The AVD has attached considerable research in recent years. Huang focused on using CMOS for logic gate design [6]. Carlson, Dewdney et al. selected a half-adder in the transcoder module and combined CMOS and pass-transistor logic (PTL) to reduce the number of transistors [7]. Jia designed a combinational logic circuit for transcoding and applied full adders to the comparator module [8]. On this basis, Jia proposed the possibility of transcoding with the truth table. However, these designs can be optimised in terms of fan-in. Du, Guo, Dong et al. increased the number of critical paths to compress the number of inputs of several logic gates [9, 10]. In fact,

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keeping the fan-in of a single gate below 4 can effectively reduce the delay. The objective of this paper is to propose a design and optimisation scheme of a 4-bit AVD, which uses truth tables and multiplexers for transcoding and focuses on the balance between delay and energy consumption. In addition, transmission gate logic (TGL) is considered for use in the structure of logic gates.

3. Design of the 4-bit AVD

This section covers the combinational logic circuit design of a 4-bit AVD. The output of the AVD should be logic 1 if the magnitude of its input signal is larger than that of the threshold level, otherwise the output is logic 0. Figure 2 shows the block diagram of an AVD.

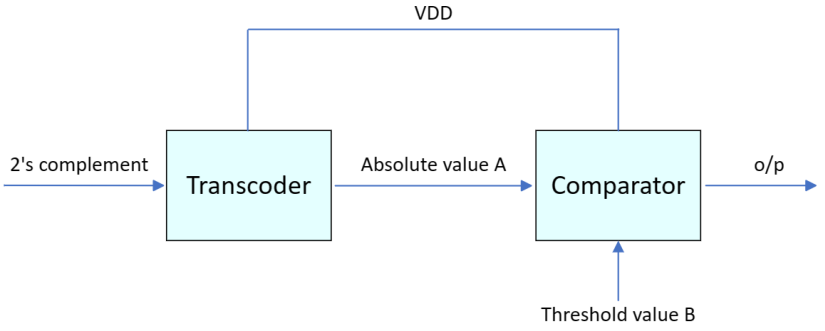

Figure 2. The block diagram of an AVD (Photo/Picture credit: Original).

3.1. Transcoder

The role of the transcoder is to identify the input signal and extract the absolute value. Since the input signal is composed of 2's complement, the most significant bit (MSB) of input signals is the sign bit, which means the input ranges from -7 to +7 in decimal. When the MSB is logic 0, the positive input number can directly enter the comparator. When the MSB is logic 1, it indicates that the input number is negative and requires to be transcoded. Table 1 shows the truth table for negative inputs [11].

Table 1. Truth table for negative inputs of the transcoder.

X_3	X_2	X_1	X_0	A_2	A_1	A_0
1	0	0	0	0	0	0
1	0	0	1	1	1	1
1	0	1	0	1	1	0
1	0	1	1	1	0	1
1	1	0	0	1	0	0
1	1	0	1	0	1	1
1	1	1	0	0	1	0
1	1	1	1	0	0	1

$X_3X_2X_1X_0$ is a 4-bit input and $A_2A_1A_0$ represents the absolute value of corresponding inputs. X_3 is 1 and it indicates negative numbers. From this table, logic functions of each output bit can be expressed as follows.

$$A_0 = X_0$$
$$A_1 = X_1 \oplus X_0 \quad (1)$$
$$A_2 = \bar{X}_2 \cdot (X_1 + X_0) + X_2 \cdot \overline{X_1} \cdot \overline{X_0}$$

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In addition, cases where X_3 is 0 are also required to be considered. For positive inputs, their absolute values are identical to the last three bits. After combining these two conditions, multiplexers are selected to detect positive or negative numbers. Figure 3 shows the circuit design of the transcoder.

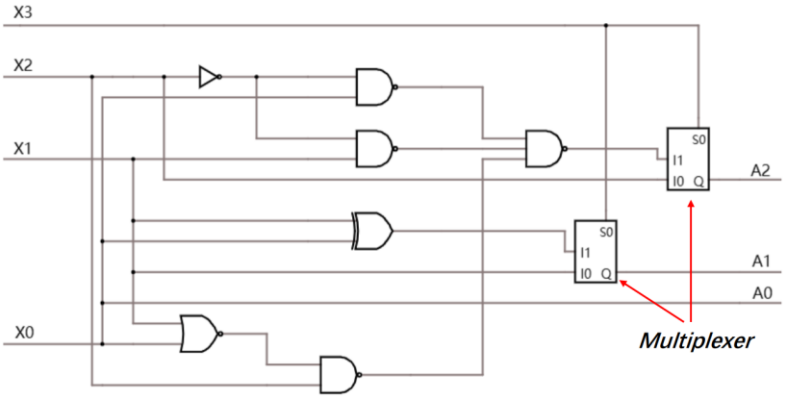

Figure 3. Logic circuit design of the transcoder (Photo/Picture credit: Original).

3.2. Comparator

The absolute value extracted by the transcoder is used as input to the comparator and then compared to a threshold value. Due to the removal of a sign bit, the comparator's input will only be 3 bits. The output should be 1 if the input is higher than the threshold level, otherwise it should be 0. Table 2 shows the design principle of this comparator and the priority of individual bits.

Table 2. Design principle of the 3-bit comparator.

A_2B_2	A_1B_1	A_0B_0	F(A>B)	F(A<B)
$A_2 > B_2$	×[a]	×	1	0
$A_2 < B_2$	×	×	0	1
$A_2 = B_2$	$A_1 > B_1$	×	1	0
$A_2 = B_2$	$A_1 < B_1$	×	0	1
$A_2 = B_2$	$A_1 = B_1$	$A_0 > B_0$	1	0
$A_2 = B_2$	$A_1 = B_1$	$A_0 < B_0$	0	1
$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	0	1

[a] It means whatever the situation is, it will not affect the final output.

$A_2A_1A_0$ is the input and the threshold value is $B_2B_1B_0$. For the convenience of comparison, the MSBs of input and output are combined to determine whether they have an impact on the outcome. The result can be expressed as follows. Figure 4 is the circuit design of the comparator.

$$F(A > B) = A_2\overline{B_2} + (A_2 \odot B_2) \cdot A_1\overline{B_1} + (A_2 \odot B_2)(A_1 \odot B_1) \cdot A_0\overline{B_0} \quad (2)$$

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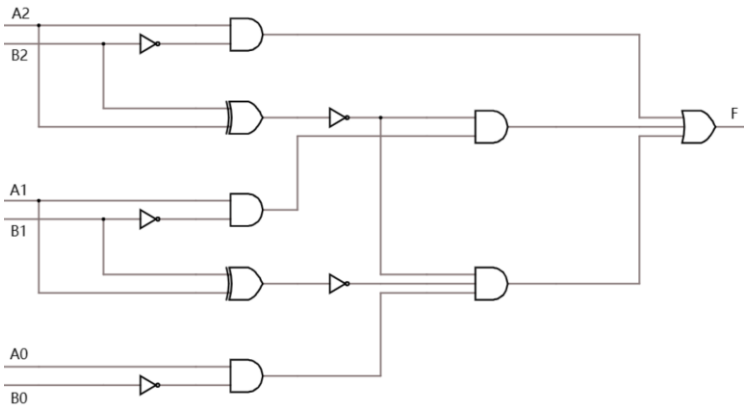

Figure 4. Logic circuit design of the comparator (Photo/Picture credit: Original).

However, it is difficult to implement simple logic AND and OR in practice, and propagation delay deteriorates rapidly as a function of fan-in. As an alternative, NAND and NOR gates are used in place of simple logic gates. After simplification, the approved design that can be produced in the industry is shown in figure 5.

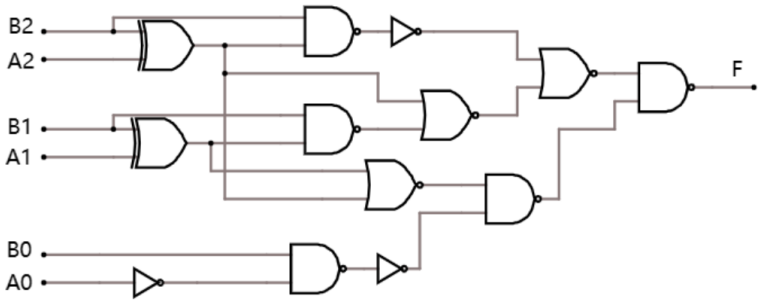

Figure 5. Approved design of the comparator (Photo/Picture credit: Original).

4. Logic implementations and Delay-energy Optimisation

In this section, technologies applied to implement the logic gates are illustrated. The delay and energy are calculated as well.

4.1. Implementations of logic gates and sizing

To obtain the longest delay of this circuit, the critical path that contains the largest number of logical gates is required. Figure 6 exhibits the critical path which contains totally 9 stages.

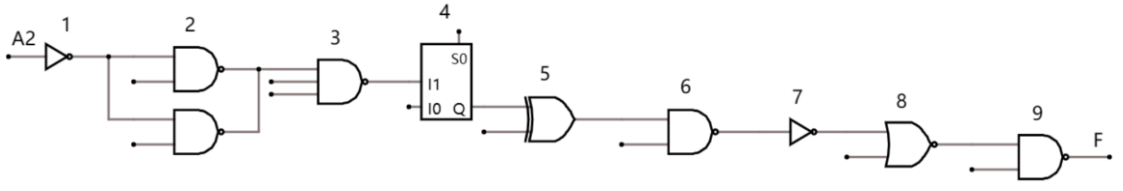

Figure 6. The critical path of the designed circuit (Photo/Picture credit: Original).

The unit CMOS inverter consists of one PMOS transistor and one NMOS transistor. The width of a PMOS transistor is 650 nm and an NMOS transistor has a width of 430 nm. Both of them have a length of 100 nm. The difference of width between PMOS and NMOS is due to the mobility of carriers. Usually, the size of an inverter satisfies the condition that the resistances of PMOS and NMOS are identical,

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which represents the same delay of these two devices. For complex gates that have multiple transistors, it is necessary to size each transistor to maintain the same delay between pull-up network and pull-down network, referring to the unit inverter.

The propagation delay is mainly caused by the charging and discharging of intrinsic capacitors in the circuit. After defining the critical path, logical effort theory can be applied to calculate the delay. For this circuit, the assumption is that the input capacitance C_{in} of every input is equivalent to 2 unit-sized inverters, and the load capacitance C_L is 32 times unit-sized inverters. The size of each transistor also reflects the capacitance. For a single logic gate, several definitions are shown below.

$$g = \frac{C_{in,gate}}{C_{in,inv}}, h = \frac{C_L}{C_{in}}, p = \frac{C_{par,gate}}{C_{par,inv}} \tag{3}$$

Where g, h, and p are logical, electrical, and parasitic efforts respectively.

Figure 7 shows the implementation of NAND and NOR gates by CMOS technology.

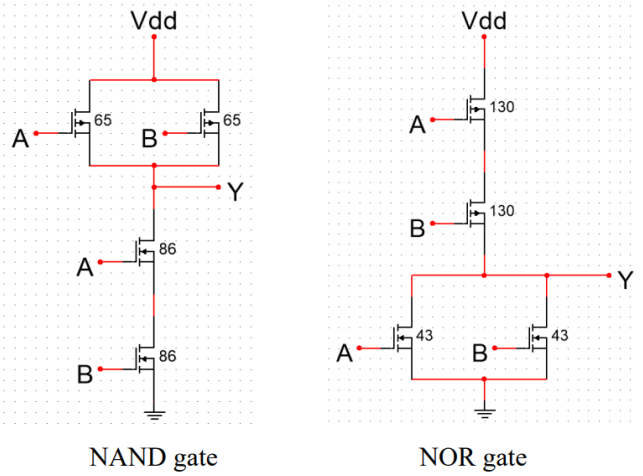

Figure 7. The implementation of NAND and NOR gates by CMOS technology (Photo/Picture credit: Original).

Figure 8 shows the implementation of multiplexers and XOR gates by TGL.

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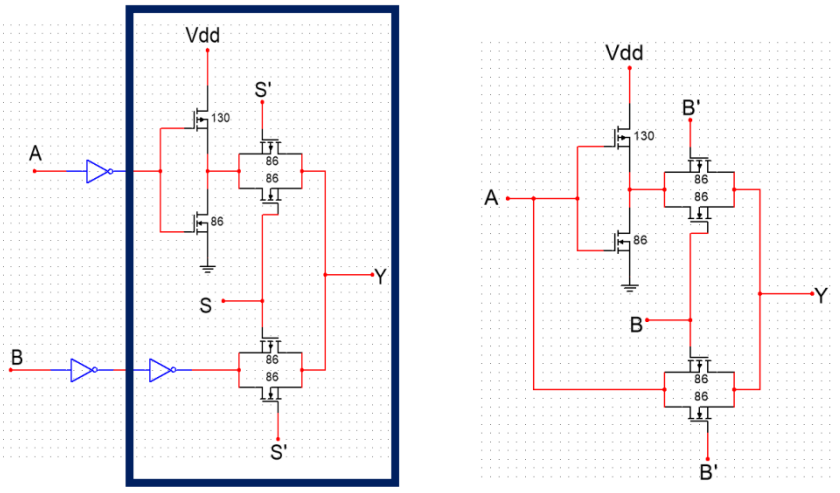

Multiplexer XOR gate

Figure 8. The implementation of multiplexers and XOR gates by TGL (Photo/Picture credit: Original).

Table 3 calculates the key parameters for delay.

Table 3. Key parameters for delay calculation of logic gates.

Logic gate	Logical effort g	Parasitic effort p
NAND	1.398	2
NOR	1.602	2
MUX	2	3.185
XOR	2.59	3.185

For the critical path, key parameters are defined as below.

$$G = \Pi g_i \tag{4}$$

$$H = \frac{C_L}{C_{in}} \tag{5}$$

Where G represents the pathway logical effort and H represents the pathway electrical effort.

Additionally, the branch path exists in the critical path and will affect the delay. The branching effort can be expressed as below.

$$b = \frac{C_{onpath} + C_{offpath}}{C_{onpath}} \tag{6}$$

$$B = \Pi b_i \tag{7}$$

$$F = GBH \tag{8}$$

$$f = \sqrt[N]{F} \tag{9}$$

Where b is branching effort, F is path effort, f is the optimal stage effort and N is the total number of stages. Therefore, the path delay can be obtained as D.

$$D = Nf + \Sigma p_i \tag{10}$$

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In terms of energy, the activity factor $\alpha_{0\to1}$ of each stage should be calculated in advance. If the output of a logic gate is Y, then the activity factor can be calculated as below.

$$\alpha_{0\to1} = P(Y=0) \times P(Y=1) \tag{11}$$

$$S = \frac{C_{in}}{C_{out}} \tag{12}$$

Where P represents the probability of the output being a zero or one and S is the stage effort. Ultimately, the energy of this path can be obtained.

$$E = \alpha_{0\to1} \times (S_i + S_{i+1}) \times C_{in} \times V_{DD}^2 \tag{13}$$

Table 4 displays the initial results with the minimum delay when V_{DD} is 1 V.

Table 4. Initial results of the minimum delay with 1 V power supply.

Stage	1	2	3	4	5	6	7	8	9
g	1	1.398	1.7962	2	2.59	1.398	1	1.602	1.398
h	2.590	1.849	1.443	1.370	1.438	1.851	2.604	1.624	1.850
p	1	2	3	3.185	3.185	2	1	2	2
S	2	2.59	4.79	6.91	5.05	2.21	4.09	10.65	17.3
$\alpha_{0\to1}$	0.25	0.1875	0.228	0.2445	0.25	0.1676	0.1676	0.2144	0.2288
D	3.590	4.585	5.591	5.926	6.909	4.587	3.604	4.602	4.586
E	1.148	1.593	3.400	3.925	2.105	1.215	2.470	6.560	12.984

The total delay is 43.98 and the energy is 35.4.

4.2. Optimisation of the delay and energy

In practice, the power consumption is an aspect that must be considered. Thus, the balance of delay and energy becomes the most critical part of integrated circuit design. For this circuit, the selected methodology is using supply voltage (V_{DD}) scaling as variables to regulate the energy-delay curve. The range of supply voltage is from 0 to 1 V. When the delay grows to 1.5 times the original, stop changing the V_{DD} and record the minimum energy at this moment. Microsoft Excel Solver can be used to simulate this model with the step of 0.05 times the minimum delay. Figure 9 is the connection between energy and delay with scaling V_{DD}.

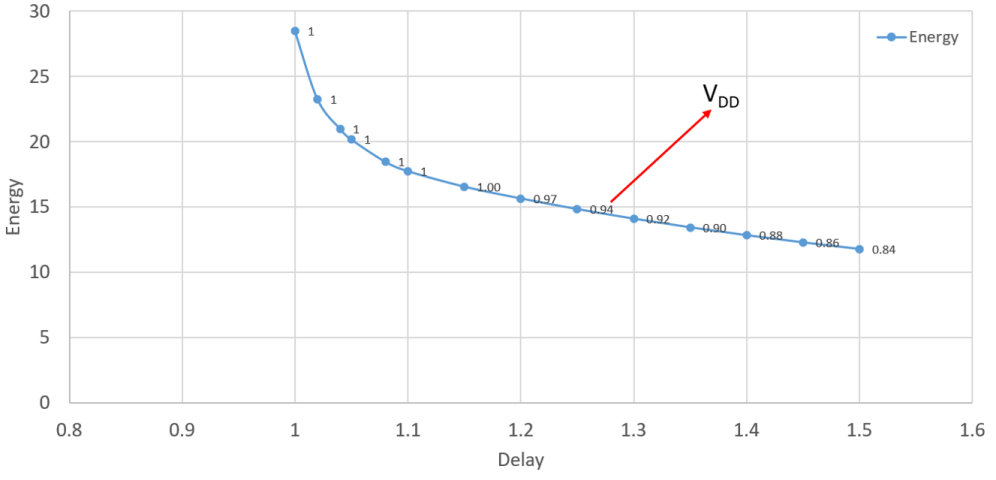

Figure 9. The relation between energy and delay with scaling V_{DD}.

(Photo/Picture credit: Original)

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Table 5 shows the comparison of initial results and optimised results.

Table 5. The Comparison of Initial Design and Optimised Design.

	Delay	Energy	V_{DD} (V)
Before scaling V_{DD}	43.98	35.4	1
After scaling V_{DD}	65.97	11.76	0.8442

It can be summarised from the table that after scaling V_{DD}, the circuit saved 67% energy and increased 50% delay.

5. Conclusion

In this paper, the structure of a 4-bit AVD was studied and designed. The logical effort theory was applied to calculate the delay and energy. The results showed that the energy consumption can be reduced by sacrificing the delay. With 1.5 times the minimum delay, this design saved 67% energy. It can be observed from the energy-delay curve that the energy consumption is suppressed with the increase of the delay. However, before the delay rises to 1.1 times, the energy decreases at a very rapid rate. Consequently, this range can bring huge benefits to the trade-off between the energy and delay.

This research provided a feasible design due to the abandonment of simple logic gates, and combined CMOS and TGL to reduce the number of transistors. Take the strict accuracy requirement of BCIs into consideration, AVDs in practical applications will certainly receive input signals far beyond 4 bits. Therefore, this design cannot meet the specifications of high-performance devices, but the research on the V_{DD} scaling is still of great significance. The development of integrated circuits is extremely fast, and the current technology has been advanced to below 100 nm. The power supply has been reduced from traditional 5 V to below 1 V. For high-level integrated chip circuits, reducing power as much as possible while maintaining performance is the primary goal. Moreover, exploring and comparing various implementations of logic gates such as bipolar CMOS (BiCMOS) is a promising optimisation methodology.

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