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A review on multiple-valued logic circuits

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Abstract. Since the traditional binary logic has several disadvantages including inaccuracy, high complexity, and limited applications. Multiple-Valued Logic (MVL), which can store more information in one digit than binary logics, require less number of logic gates and take the third value in practical logic problems, is developed and introduced. More information stored per digit leads to higher computational efficiency. Less logic gates results in more spaces on the circuit board. Considering the third value means higher accuracy. In this research, some examples of different MVL circuit are designed to give a rough picture of current research in this domain. These designs are based on ternary and quaternary logics rather than binary logics. Besides, reliability evaluation through mathematical approach is presented in order to prove that the new design is more preferable. This can be carried out with mathematical analysis such as calculating a matrix that reflects its reliability, and simulating different designs to obtain certain values and comparing them with each other. Despite facing various challenges, including complicated physical implementation and difficulty to modulate the signals. This means that there is still potential of further research in this domain of logic circuits. This result in the conclusion that the MVL logic circuits will replace the conventional binary logic circuits in the future, and probably that decimal logic would be developed and no binary-to-decimal conversion unit will be required.

Keywords: Multiple-Values Logic, Electronics, Computer Science.

1. Introduction

Multiple-Valued Logic (MVL) refers to a propositional calculus that encompasses logical values beyond the traditional binary distinction of 'true' and 'false'. This subject possesses a lengthy and culturally significant chronology that may be traced back to the era of Ancient Greece. In the year 1920, the Polish philosopher Łukasiewicz put up a proposition to expand the functionality of binary Aristotelian logic, which was limited to two values: true and false [1]. Additionally, the American mathematician Post introduced his own multi-valued versions of operators, namely AND, OR, and NOT, which allowed for conjunctions, disjunctions, and cycles [2]. In a subsequent publication in 1928, Bernstein highlighted that the modular operations encompass the operations of modulo-p addition and multiplication on the set of integers modulo-p [3].

Initially, researchers in the field of microelectronic circuits focused on achieving cost efficiency by using multi-valued processing in basic operations. As an illustration, a logic gate that encompasses four distinct values for inputs, outputs, and function have the capability to execute the equivalent of two bits each operation. The objective is to achieve physical implementation of this logic by constructing a gate or a whole system at a reduced expense, wherein the binary function is executed using traditional logic

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gates that carry out an equivalent operation. The complexity of this issue is heightened by several factors. In earlier circuit technologies, multi-valued logic (MVL) gates frequently exhibit lower noise margins, lack tolerance to specific process fluctuations, and pose challenges in terms of electrical restoration [4].

However, it is worth noting that the ideas that form the foundation of multiple-valued logic have given rise to various significant developments, as evidenced by the content of this paper.

This paper provides a comprehensive examination of multiple-valued logics, with particular emphasis on their physical implementation and potential future developments. It will analyse and summarise recent research on integrated circuits that utilise multiple-valued logic techniques.

2. Circuit Design Techniques and Examples

There exist two primary methodologies for designing Multiple-Valued Logic (MVL) systems: one is grounded in current, while the other is grounded in voltage. Babu et al. (2003) introduced a design methodology for the latter. To begin with, the objective is to transform a binary function into a quaternary function, while maintaining the presence of two distinct values. Furthermore, the process of pairing the obtained functions can be considered. Thirdly, Implement the functions coupled together in one circuit with transistors. The suggested method differs from the standard method in that it utilises only half of the output pins without delay, resulting in improved efficiency in function realisation. However, it is important to note that the proposed method generally necessitates a greater number of transistors [5].

In a study conducted by Rosenman (2016), an alternative methodology was proposed for the verification and analysis of digital hardware designs. This approach builds upon the existing ternary or quaternary simulation methods by including MVL. The simulations conducted in the context of the more informative MVL scenario provide insights that may not be observed or may be more challenging to identify in binary and ternary simulations. In the context of equivalence verification, the identification of distinct behaviours during MVL simulations can be helpful in uncovering either a true binary non-equivalence or a qualitative disparity between two systems. The variable's value in a simulation may encompass data pertaining to its veracity and its origins in terms of both location and time. Applications of this technology encompass several areas such as equivalence verification, initialization, production and verification of assertions, partial control over data flow, and prioritising and block-oriented simulations. The majority of this research focuses on the theoretical components underlying the MVL approach. This includes an examination of the rationale for using a certain algebraic framework for calculations, as well as the introduction of concepts such as the DeMorgan canonical form and the verification complexity of Boolean expressions. This paper introduces two fundamental algorithms that utilise simulation techniques. The first approach is designed to satisfy and verify combinational designs, while the second algorithm focuses on confirming the equivalence of sequential designs. The user's text is already academic and does not need to be rewritten [6].

The described framework, which was presented in a different study by Jaber et al. (2022), consists of three ternary combination circuits, six Ternary Arithmetic Logic Units (TALU), and eight ternary logic gates. The ternary logic gates comprise a set of seven unary operators operating within a three-valued system. The operators encompassed in this set are denoted as A^1, A^2, $(A^2)^{-}$, A_1, $1.(A_n)^{-}$, $1.(A_p)^{-}$, and the Standard Ternary Inverter (STI) A^{-}. Furthermore, it is worth noting the existence of the ternary NAND gate, which operates on the principles of Carbon Nanotube Field-Effect Transistors (CNFETs). Ternary combinational circuits consist of two unique designs for Ternary Decoders (TDecoder) and Ternary Multiplexers (TMUX). TDecoder1 utilises unary operators that are reliant on Complementary NanoFETs (CNFETs), whereas TDecoder2 employs binary gates that are based on Double-Pass Logic (DPL). In addition, TMUX contains the usage of CNFET-based unary operators, as proposed in the literature. Ternary Arithmetic Logic Units (TALUs) consist of three distinct designs that are relevant to Ternary Half-Adders (THAs) and Ternary Multipliers (TMULs). The initial design comprised the recommended TDecoder1, STI, and TNAND elements. The second design integrates the intended cascading approach of TMUX. With respect to the third design, it integrates the proposed unary operators and TMUX. This design effectively balances the trade-off between transistor count and energy

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efficiency through the implementation of strategies such as the utilisation of transmission gates and the utilisation of dual supply voltages. The simulations provide evidence that the proposed designs showcase a significant decrease of 73% in the quantity of transistors need for the THA. Furthermore, notable reductions in energy consumption up to approximately 88%, 99%, 98%, 84%, 98%, and 99% are observed for the STI, TNAND, TDecoder, TMUX THA, and TMUL, correspondingly. In addition, the secondary aim is to utilise ternary data transmission as a method to improve the effectiveness of data interchange between computer hosts. Furthermore, the research paper introduces a bi-directional circuit that consists of two converters, especially a binary-to-ternary converter and a ternary-to-binary converter [7].

3. Evaluation

There are various methodologies for assessing the dependability of a binary logic system. One approach involves the utilisation of matrices to depict a constant probability associated with the occurrence of an error. Abbasinasab and Yanushkevich (2012) employed the "matrix-based method" to investigate the application of this approach in a multi-valued logic (MVL) system. The utilisation of a mathematical construct known as the Probability Transfer Matrix (PTM) is implicated. The signal error probability refers to the likelihood that a signal deviates from its accurate value and assumes an erroneous value. The value is derived by summing the probabilities of all potential errors. The gate error probability refers to the likelihood that a gate would provide an erroneous output rather than the expected output. The achievement is obtained by summing the probabilities of all possible outcomes generated at the output of the gate [8].

In a paper about multiple-valued logic gates implemented with pseudo N-type carbon nanotube field effect transistors (CNTFETs) and without resistors by Jiang et al., the evaluation is carried out by comparing several figures of merit, such as power consumption, propagation delay, power-delay product, and circuit area of different designs, namely resistor-loaded MVL, complementary MVL and N-type CNTFET Standard Ternary Inverters. The values are obtained from computer simulation [9].

4. Applications

The implementation of MVL in the context of fuzzy control entails the usage of a set of if-then rules that dictate the system's response to external stimuli originating from the environment. As per the reference supplied [10]. The utilisation of MVL in the field of quantum optics is widely acknowledged as a dependable methodology for network quantum key distribution, which holds promising implications for the establishment of secure distributed quantum computing systems. Furthermore, it is imperative for MVL to provide cryptographic safeguards for mobile robots and the Internet of Things (IoT) in forthcoming times. The successful execution of this undertaking requires the creation of innovative cryptographic encoding mechanisms, which could potentially integrate concepts of multi-valued logic. However, this specific logical framework offers new possibilities for the hierarchical clustering of various datasets. The examination of aggregated entities can be enhanced by utilising the minimization of multiple-valued logic functions, a methodology that can be implemented for any given number of variables. The suggestion recommends the adoption of a heterogeneous network design in order to effectively exploit the advantageous characteristics of multiple-valued logic. This architectural framework has three separate levels of artificial intelligence logic modelling, each tailored for discrete multiple-valued logic, Boolean logic, and fuzzy logic, respectively. The utilisation of multiple-valued logic is widely acknowledged within the academic community as a promising foundation for the implementation of additional levels of encryption, data consolidation, and communication capabilities. This capability is achieved by the utilisation of a cohesive high-dimensional space for network addressing and the precise manipulation of robotic devices. The classification of Boolean and fuzzy logic models into several levels of logic is undertaken in order to ease the integration of various algorithms and facilitate the administration of additional data protection measures. The phrase "means for robotic agents" pertains to the techniques or procedures employed by robotic agents in order to achieve their tasks or goals [11].

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In addition, the use of quantum technologies and the incorporation of artificial intelligence techniques like as neural networks and multi-agent systems are assumed in position-based cryptography schemes for network mobile robots. The simplification of the design of these schemes can be achieved by the utilisation of MVL, which is employed for both the modelling of the position-based cryptography protocol by the neural network. This approach allows for an increased range of verification methods. The user's text does not provide any information to rewrite in an academic manner [12].

In their study, Shmerko et al. (2023) identified a novel domain where advanced MVL can be applied: the collaboration between humans and self-disciplined machines within rapid response teams such as firefighters, search-and-rescue operators, disaster response personnel, and military special operations forces. The research team has devised a specific approach for formalising cooperation protocols, often referred to as contagion protocols, which serve as models for the collaboration between humans and machines in emergency missions. MVL approaches effectively meet the criteria for encoding the states of stress and trust, as well as facilitating their propagation across team members. Additional valuable uses of advanced MVL approaches encompass the modelling of various phenomena, including the propagation of infectious diseases, as well as the dissemination of rumours, ideas, panic, and terror [13].

5. Conclusion

Since the conventional two-valued logic is constraint by its disadvantages such as low accuracy, highly complicated structure and narrow range of application, it will be gradually replaced by MVL which can overcome such issues. Devices with MVL technologies will have higher operational efficiency, smaller size of the circuit board, higher accuracy, and lower energy consumption. As the form of the society is evolving towards the higher form, higher degree of productivity is necessary. To increase productivity, the technology requires essential innovations, and MVL will probably be one of them.

Despite that, MVL technology is yet to be mature enough to be applied widely, which the cases mentioned in this paper have proven. Most of the MVL technology are merely theories and have not been applied in daily usage yet at present. Additionally, complicated physical implementation and difficulty in moderating signals hinder the development of this technology. This paper ignores an important determinant fact, which is semiconductor materials, leaving inaccuracy of this paper.

It is possible that ternary and quaternary computers will be developed and be widely used in computer in the following century, enhancing the functionality of the computer. In the further future, decimal logic in electronics will be developed and applied so that the logic conversion unit will no longer be required.

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