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Exploring the significance and applications of Field Programmable Gate Arrays in modern integrated circuits

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Abstract. In recent years, the rapid advancement of electronic technology and large-scale integrated circuit technology has led to increased integration of integrated circuits and expanding system scales on integrated motherboards. This evolution presents new challenges and demands in system design. Field Programmable Gate Arrays (FPGAs), a vital VLSI technology, have found extensive applications in communication, image processing, computers, and other domains, becoming a pivotal component of contemporary electronic systems. This paper aims to enhance the understanding of FPGAs by first delving into their theoretical foundations, followed by an overview of their general structural elements and a historical perspective on FPGA development. Additionally, this analyse and summarize relevant literature in the third section, focusing on the three primary application areas of FPGAs, elucidating their research processes and findings. Finally, the fourth section offers insights into the future directions of FPGA development, grounded in the current context. By acquainting readers with FPGA's essential attributes and its multifaceted applications, this paper underscores the pivotal role of FPGAs in the landscape of modern integrated circuits.

Keywords: FPGA, Integrated Circuits, System Design, VLSI Technology.

1. Introduction

In recent years, with the fast development of electronic technology and large-scale integrated circuit technology, the integration of integrated circuits is getting much tighter, and the system scale on the integrated motherboard is also constantly improving, which also brings new requirements for system design. As a kind of Very Large Scale Integration (VLSI) technology, the communication field has extensively used programmable gate array, image processing, computer, and other fields, and is the most important part of the current electronic system.

In order to better understand FPGA, the second part of this paper first introduces the theoretical basis of FPGA, then summarizes the basic structure of the general FPGA, and finally reviews the development process of FPGA since its birth. At the same time, in the third part, according to the three main application areas of FPGA, Relevant literatures are selected and their research process and conclusions are analysed and summarized. Finally, in the fourth part, the future development direction of FPGA is predicted based on the current actual situation.

Through the introduction of the essential characteristics of FPGA and the analysis of its application in different fields, I hope to help readers better understand what FPGA is, and realize the important

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position of FPGA in today's integrated circuits, and then inspire researchers to carry out innovative research on FPGA from different angles, so as to promote the further development of FPGA.

2. Theoretical basis analysis of FPGA

2.1. Brief definition and characteristics of FPGA

To address the drawbacks associated with custom circuits and surmount the limitations imposed by gate quantities in original programmable devices, the Field-Programmable Gate Array (FPGA) emerged as a semi-custom circuit within the domain of Application-Specific Integrated Circuits (ASIC) [1]. In essence, FPGA represents a chip capable of altering its internal configuration to align with users' requirements. To achieve this, individuals need to devise a hardware description language through programming, subsequently harnessing Electronic Design Automation (EDA) tools. These tools prove invaluable in pivotal processes such as functional design, synthesis, verification, and more, significantly aiding researchers in the completion of Very Large-Scale Integrated Circuit (VLSI) chips. Following compilation, the resulting layout and wiring are compiled into a file and then burned onto the FPGA device. Ultimately, this process facilitates the modification of the FPGA's internal connections, enabling the realization of desired functions. FPGA offers a multitude of advantages, including:

(1) FPGA is composed of different hardware. The realization of its complex functions requires reasonable organization and configuration of these hardware.

(2) Humans can simply use block diagram or Verilog HDL to design FPGA, which improves the logical rationality of FPGA design, while reducing the degree of design difficulty, and is conducive to the understanding and application of other users.

(3) Because of EDA tools, the FPGA can be infinitely reprogrammed, it only takes hundreds of milliseconds to load a new design, and using reconfiguration means the cost of hardware won't be so high.

(4) FPGA chip and design can directly influence the working frequency, and sometimes when it meets some stringent requirements this character can be modified by faster chips.

2.2. Composition structure of FPGA

The programmable nature of FPGAs allows for the creation of digital logic structures that differ from fixed ASIC circuits. To achieve this programmability and configurability, FPGAs require a structure that can be repeatedly reconfigured. This need for repeatable programming and configuration is effectively met by lookup tables (LUTs), which are the foundation of today's mainstream FPGA chips, primarily utilizing SRAM technology [2].

A LUT, essentially an SRAM module, stores data in a manner similar to a truth table. It employs two components resembling a truth table to replace the inputs and outputs of logical operations. In practice, it utilizes input data as an address within the SRAM, retrieves the corresponding value based on the address, and then outputs this value as the result. Figure 1 illustrates how LUTs, in conjunction with registers, form the fundamental building blocks of the logic structure.

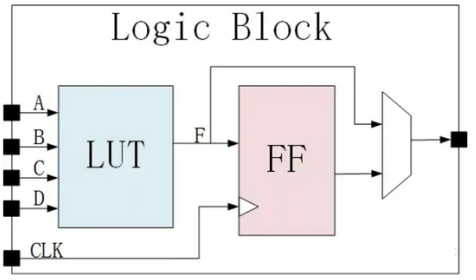

Figure 1. Basic structure of the logic block [2].

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An FPGA typically comprises six key components, which are as follows: Programmable Input Output Unit (IOB), Basic Programmable Logic Unit (CLB), Comprehensive clock management module, Abundant cabling resources, Embedded block RAM, Embedded foundational functional units, and Embedded dedicated hard cores. The fundamental architecture of the FPGA is depicted in Figure 2.

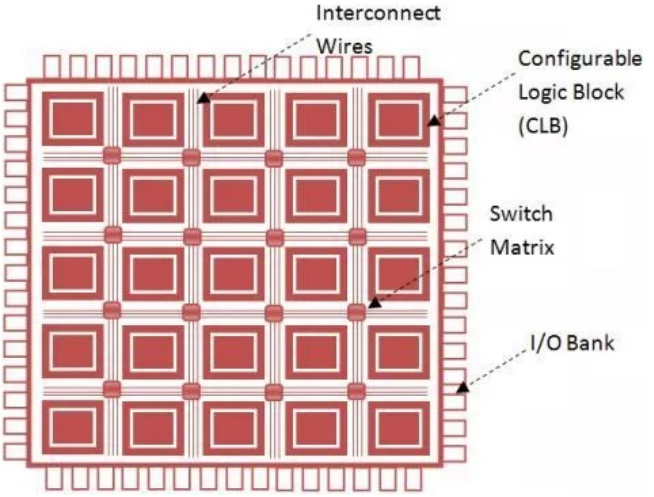

Figure 2. Basic structure of the FPGA [2].

2.3. Historical development and current situation of FPGA

From the appearance of FPGA in 1984 until today, its development is inseparable from the innovation and development of process technology and the transformation of application requirements. The development of FPGA can be divided into four stages:

(1) 1984-1991 - Invention era

During this era, the number of available FPGAs was considerably smaller compared to the demands of user application products. Consequently, multi-FPGA systems gained popularity, and the development of automated multi-chip partitioning software became a critical component of FPGA design suites. The distinctive FPGA architectures made it impossible to create a one-size-fits-all design tool, leading FPGA vendors to take on the responsibility of developing Electronic Design Automation (EDA) tools tailored to their specific devices. Due to constraints on on-chip wiring resources, manual design and optimization often became necessary to address design challenges [3].

(2) 1992-1999 – Expansion era

In the early 1990s, the FPGA startups often didn't have access to cutting-edge chip technology without fab. FPGAs thus lagged the development of IC. By the late 1990s, IC founds realized that FPGAs were an ideal enabler can remove the obstacles to process development. Each new generation of the process doubles the number of transistors, halves the cost per function, and doubles the size of the largest FPGAs. The main features of this phase are as follows: chip area is less important, automated design is beginning to gain more attention, SRAM is emerging as the preferred technology, and LUTs start to be used as logic cells.

(3) 2000-2007 -- Accumulation era

As chip capacity and design complexity have grown, the FPGA has found significant opportunities in the communication industry. However, expanding capacity alone is not sufficient for market growth. Instead, two strategies have emerged: 1. Low-End Market Focus: In the low-end market segment, manufacturers have shifted their attention towards enhancing efficiency and producing cost-effective FPGAs. 2.Facilitating FPGA Utilization: On the other hand, FPGA vendors are striving to simplify the use of larger FPGAs by developing soft logic libraries. These libraries make it easier for customers to harness the capabilities of the largest FPGA devices.

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During the 2000s, FPGA users faced the challenge of aligning their designs with system standard requirements. These standards were essential for connecting external components or facilitating internal module communication. Consequently, FPGAs evolved into complex function sets integrated with programmable logic.

(4) 2007-present -- System era

To address system design challenges, FPGAs are now incorporating various systematic modules, including high-speed transceivers, memory units, DSP processing capabilities, and more. Moreover, essential control functions such as bitstream encryption, verification, mixed-signal processing, power and temperature monitoring, and power management are being integrated into FPGA devices. These features are prominently showcased in the Zynq All-Programmable device.

Furthermore, the development of these devices has driven advancements in programming tools. System FPGAs demand efficient system programming languages, and options like OpenCL and C languages are now available for programming FPGAs in a manner that resembles software development processes.

3. Analysis of application scenarios based on FPGA

3.1. Communication System

In wireless communication systems, many function modules usually require a large number of filtering operations, by implementing the distributed arithmetic architecture in FPGA, these operations can be implemented efficiently. The current wireless communication field is developing towards the combination of audio and information. On the other hand, it is pressing to combine mobile technology into handheld PDA products. Therefore, with the progress of wireless mobile communication system, and the anticipation of better portable system, the system module's processor must be more powerful. Some important challenges are raised to the market of FPGA chips for wireless communication by these requests. It is widely known the power consumption, performance, and cost are three vital factors and this is why many researchers try to balance these three demands.

As in the paper "ON-FPGA COMMUNICATION ARCHITECTURES AND DESIGN FACTORS", the authors note the great computational potential brought by the development of current platform FPGAs and system-on-field-programmable chips architectures [4]. However, it is also found that with the increase of the number of embedded processors, the communication bandwidth between components will affect the overall system performance. Therefore, the authors investigate and evaluate the current mainstream FPGA communication architectures, and design quantitative performance indicators and qualitative factors for analysing the characteristics of different architectures. This paper hope to find the best communication architecture and inspire the innovation of foreign FPGA communication. In this paper, the author first classified the most advanced on-chip communication architectures: point-to-point interconnection, bus architecture, Network on chip (NoC), and their advantages and disadvantages. The Categories of on-chip communication is shown in figure 3.

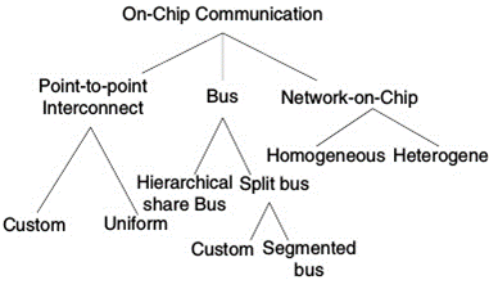

Figure 3. Categories of on-chip communication (Photo/Picture credit: Original).

In "Design and FPGA-Based Realization of a Chaotic Secure Video Communication System", The author chooses FPGA as a platform to realize a chaotic secure video communication system [5]. Because

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humans are in an era of big data, with massive, strong real-time characteristics, so the traditional encryption algorithm is difficult to real-time encryption, so the author developed the image and voice encryption algorithm based on chaos according to the principle of anti-chaos control. The cryptographic algorithm based on chaos relies on the complex dynamics and deterministic nonlinear mapping of continuous-time dynamical systems. This paper introduces two implementation schemes, one is hardware implementation based on FPGA platform, the other is software implementation based on ARM platform. Because the FPGA method is based on logic cells or basic gates, it can take full advantage of the parallel processing of FPGA. Hardware experimental results show that the proposed method has a fast execution speed suitable for real-time video processing. The authors design a 6-dimensional discrete-time RDCS chaotic system based on Verilog HDL hardware implementation, and develop the corresponding Verilog HDL algorithm. This paper also introduces how to use the system for real-time video encryption and decryption, and uses TESTU01 test suite to test the security of the system. Finally, the paper points out three advantages of the proposed system over the existing designs: better statistical performance, higher security and better test results.

3.2. Digital signal and video image processing

Because of the high-speed parallel ability of FPGA, the chip can complete a variety of tasks with multiple threads at the same time, so the parallel architecture can be used to realize the function of digital signal processing. What's more, its interface voltage and drive capability are programmable configurable unlike the traditional DSP. In addition, the image quality continues to improve, which makes the processing chip needs to process more and more data in real time, and the compression algorithm is more and more complex, so that the use of ASSP or DSP unable to meet such a large amount of data processing. Then the advantage of FPGA is highlighted, it can be more efficient to process data, after considering the cost, FPGA is also more and more popular in the market.

In the "Implementation of Real Time Image Processing System with FPGA and DSP" published by M V Ganeswara Rao et al., the author made FPGA and DSP to work together to achieve a real-time image processing system, using Xilinx FPGA chip as the image sampling and display control unit, the following figure 4 shows the system structure diagram [6].

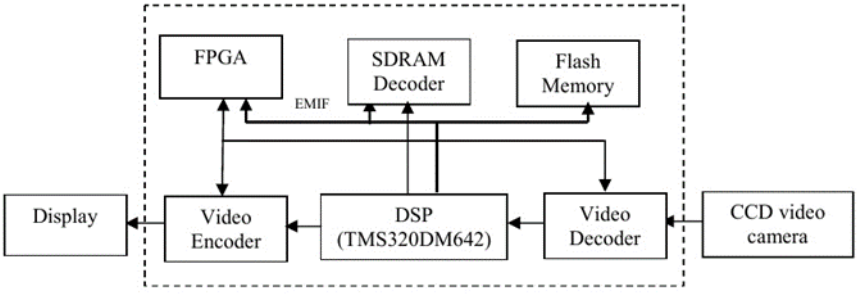

Figure 4. The diagram of system structure [6].

FPGAs play a vital role in the system by capturing and presenting intricate images, and their specific functions are outlined below: EMIF Interface: FPGA serves as the interface bridging connections between DSP, SDRAM, flash memory, and itself. This is depicted in Figure 4. DSP Processor Activation: The DSP processor activates CE0, CE1, CE2, and CE3 signals, which are then routed to the child card interface connectors, as detailed in Table 1.

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Table 1. Functions of different chip select.

Chip Select	Function
CE0	SDRAM bus
CE1	8 bit Flash, UART, FPGA functions
CE2	Daughter Card Interface
CE3	FPGA Sync Registers Daughter Card Interface

The FPGA chip offers a versatile set of features, including 10 asynchronous memory registers that can be activated using CE1 for multiple functions. Additionally, it employs synchronous registers for sampling and display control, which are governed by CE3. Moreover, it incorporates the following components: 1. An address decoder for seamless interaction with EMIF. 2.Register files encompassing both synchronous and asynchronous registers. 3.An OSD data FIFO with a 256-word capacity and 32-bit width.

The Sobel edge detection algorithm was employed for validation purposes. To implement the DSP function, Code Composer Studio 3.1 was utilized, while the FPGA function was implemented using Xilinx 12.2 IDE. The experimental outcomes demonstrate that the system can efficiently capture video frames at a rate of 25 frames per second and perform real-time processing and display. Furthermore, the system exhibits robust performance across various lighting conditions and complex backgrounds, showcasing its adaptability to accommodate diverse computation-intensive image processing algorithms.

In the paper titled "A Novel FPGA/DSP-Based Parallel Architecture for Real-Time Image Processing" (Reference [7]), the primary focus is on introducing a parallel architecture that combines FPGA and DSP technologies to achieve real-time image processing. This architecture emphasizes the integration of DSPs using FPGA as an intermediary, along with the implementation of a FIFO-based interconnection network and a specialized data communication protocol within the FPGA.

Figure 5 in the paper illustrates this innovative architecture. It depicts the arrangement in which three DSPs (specifically, C6414 DSPs) are interconnected by FPGA components. Each individual DSP is linked to the FPGA through EMIFA (External Memory Interface A) and engages in data exchange with the other two DSPs via a sophisticated FIFO network established within the FPGA.

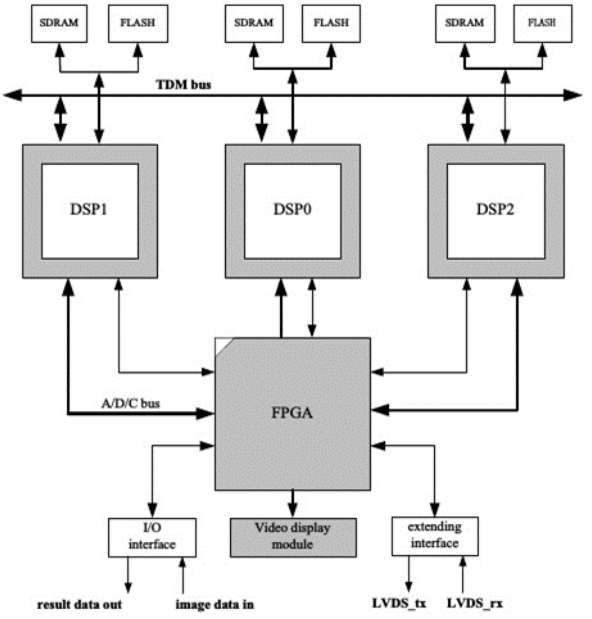

Figure 5. The new architecture based on DSP and FPGA [7].

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A significant contribution highlighted in this paper concerning FPGA technology is the establishment of an inter-DSP connection network incorporating FIFO pathways and a tailored data communication protocol, as illustrated in Figure 6. This network is designed to facilitate efficient data exchange between the DSPs and is realized within the FPGA framework.

For each DSP unit, there are two distinct FIFO groups, enabling bidirectional data communication with the other two DSPs, respectively. These FIFOs are implemented using the embedded memory available in the Altera Stratix FPGA and are configured with specific depths to accommodate the data requirements. Furthermore, the FIFO control interface plays a pivotal role in managing the glue logic for the FIFOs. This interface handles essential functions such as address decoding, read-write timing adjustment, and communication handshake, ensuring seamless integration with the DSP units.

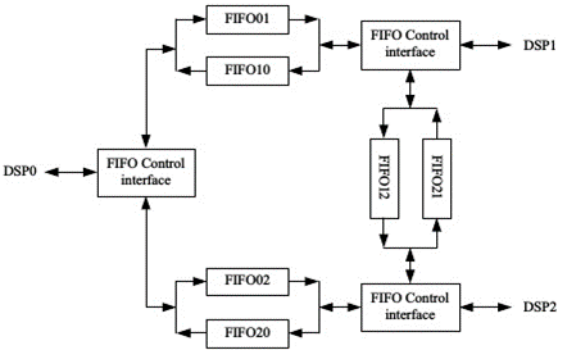

Figure 6. The structure of connection between DSP and FIFO [7].

The performance evaluation of the architecture in the prototype system is also presented, including the performance of data communication between DSPS and system computing power. The experimental results show that the architecture has high data transmission bandwidth (up to 400MB/s) and low latency, and it also has high image processing performance.

3.3. Artificial intelligence

AI is considered to be an important driving force for a new round of scientific and technological revolution and industrial change. Therefore, various AI algorithms emerge in an endless stream, which provides a stage for FPGA which has a very high degree of parallelism. In deep learning, many computations can be parallelized, such as convolution and pooling operations. The parallel computing ability of FPGA can make the acceleration of deep learning algorithm on hardware more obvious. Secondly, FPGA has low latency and high bandwidth. In deep learning, the training and inference of the network require a large amount of data transmission and computation, so low-latency and high-bandwidth hardware devices can accelerate the whole process. FPGA can achieve efficient data transmission and computation through customized data flow architecture.

Zhengjie Li et al., in A survey of FPGA design for AI era, conducted a survey on a series of FPGA chip designs for AI, mainly discussing the design of DSP module, ALM module, CLB module and memory module [8]. As well as new architectures and specialized AI engines. The article points out that reconfigurability, customizable data flow and data width, low power consumption and real-time performance make FPGAs an attractive platform for accelerating CNNS, but at the same time, the computation and memory resources of FPGAs will be the limiting factors, so various researchers and enterprise developers have spent a lot of effort to redesign FPGAs. Therefore, various researchers and enterprise developers have spent a lot of efforts to redesign FPGA chips to better meet the development needs of DNN. Among them, the design of DSP module includes supporting low-precision operation and supporting floating-point multiplication and accumulation (MACs) operation. The ALM module was designed to support low-precision MACs and BNN (binary neural network) operations. The design of storage module includes embedded memory, HBM (high bandwidth memory) in package and off-line memory interface.

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4. Future development trend of FPGA

As semiconductor technology advances rapidly, FPGA devices, serving as highly efficient reconfigurable integrated circuit platforms, have witnessed substantial improvements in performance and system integration. Concurrently, new directions have emerged [9].

Firstly, with the integration of chip giants, FPGAs will be further integrated with traditional chips, giving play to their programmability advantages, empowering traditional chips with new capabilities. The widespread use of data centres has led to an increase for processing power for important tasks, including network control and security, and major chip companies have come up with their own solutions. At present, it is not the best solution to launch FPGA products only, but to launch new chip categories by integrating FPGA with other chips.

Looking at it technically, the future of FPGAs holds the promise of enhanced integration and connectivity on two distinct tiers. Firstly, FPGAs offer unmatched flexibility, but for common modules, their efficiency falls short. Consequently, the prevailing approach will continue to be the integration of hard IP directly onto the FPGA chip. This strategy caters to the requirements of both efficiency and adaptability, establishing itself as the dominant concept. It will further bolster FPGA functionality and enable its penetration into fresh application domains [10]. The second tier involves the integration and connectivity of FPGAs with other chips within the broader system context. The author contends that this level of integration is pivotal for FPGAs to empower novel chip systems and categories, thereby unlocking new opportunities in the market.

The future evolution of FPGAs will crucially depend on software development. With FPGAs increasingly intertwined with other chips, ensuring that software can fully harness their potential while circumventing scheduling bottlenecks emerges as a complex yet vital concern. This complexity arises from the potentially stark differences in programming models between FPGAs and other system components, such as CPUs. It is firmly believed that as FPGAs assume a pivotal role in the emerging system-on-chip landscape, a corresponding software ecosystem must keep pace. Only through this alignment can this new paradigm of FPGA systems genuinely achieve mainstream adoption.

5. Conclusion

From the application analysis of FPGA, it can be concluded that FPGA is widely used in the fields of communication, image and AI, and the flexible transformation characteristics of FPGA make it suitable for the large amount of information and complex environment in the era of big data. Secondly, because the data are real-time and relevant, the research based on FPGA is inseparable from the analysis of the processing speed of the task. In addition, the chip area and power consumption also need to be highly continuous attention. Finally, from the examples of various applications of FPGA, it can be seen that the current research is to use various types of chips to coordinate work, and use the advantages of different chips to make up for the shortcomings in order to further improve the overall performance.

The analysis of the future development trend of FPGA from the perspective of FPGA market and its own hardware and software development. FPGA will integrate more IP, and then integrate with other chip types, and then be controlled by a unified software algorithm, which reduces the burden of algorithm engineers and is more conducive to users to understand the principle. Therefore, it can achieve more complex functions and meet the diverse requirements of human beings.

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