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The application of Verilog in the development of casual games

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Abstract. Verilog is a hardware description language (HDL) that is widely used in digital circuit design and simulation. Its development is closely related to computer science and electrical engineering. Verilog gained popularity in the early 1980s as digital circuit designs became increasingly complex, requiring more efficient circuit design and verification tools. At the same time, rapid advances in computer hardware also stimulated the demand for digital circuit design languages. Furthermore, the popularity and adoption of Verilog highlight the growing necessity for digitisation, automation, and intelligence in modern society. As digital technology continues to advance across various industries, the need for effective and dependable digital circuit design languages is also increasing. This paper delves into the complex process of recreating the timeless arcade classic Pac-Man on the Spartan 3E FPGA platform using hardware description and digital circuit techniques and the Verilog programming language. Through a comprehensive review of existing literature and research, this study investigates the fusion of traditional game design principles with state-of-the-art hardware programming methods, demonstrating the seamless integration of software-driven game mechanics with hardware-based implementation. Through careful design and coding strategies, Pac-Man's basic functionality, such as maze traversal, ghost AI, and pellet consumption, is faithfully replicated using Verilog modules customized for the Spartan 3E FPGA board. By bridging the realms of game development and hardware engineering, this paper not only showcases the versatility of Field Programmable Gate Array (FPGA) technology in entertainment applications but also underscores the interdisciplinary nature of modern computing endeavours.

Keywords: Pac-Man, Verilog, FPGA, Game development.

1. Introduction

The realm of digital entertainment has witnessed a remarkable evolution since the inception of arcade gaming, with classic titles like Pac-Man captivating audiences worldwide [1]. As technology progresses, the opportunity arises to explore the convergence of traditional gaming experiences with modern hardware programming paradigms. This thesis embarks on a journey to merge the nostalgic charm of Pac-Man with the sophistication of Verilog programming language, targeting the Spartan 3E FPGA platform for implementation.

Pac-Man, an iconic arcade game introduced in the early 1980s, remains a timeless emblem of gaming culture, renowned for its addictive gameplay and distinctive characters [2]. The objective of the game is simple yet engaging navigate the titular character, Pac-Man, through a maze while avoiding ghosts and consuming pellets. This simplicity belies the intricacies of game mechanics and level design that

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have made Pac-Man a perennial favorite among gamers of all ages. In recent years, the field of hardware description has emerged as a powerful tool for designing complex digital systems, offering unparalleled flexibility and efficiency in hardware design [3]. Verilog, a hardware description language widely used in the industry, provides a robust framework for describing digital circuits and systems.

The choice of the Spartan 3E FPGA platform for this paper stems from its versatility and affordability, making it an ideal candidate for prototyping and experimentation [4]. Field Programmable Gate Array (FPGA) technology offers the unique advantage of reconfigurability, allowing developers to iterate and refine their designs with ease. This paper seeks to explore the intersection of game design principles with hardware programming methodologies, unravelling the intricate interplay between software-based gameplay logic and hardware-based execution. By delving into the complexities of FPGA-based game development, this paper hope to shed light on the challenges and opportunities inherent in bridging the gap between virtual entertainment and physical hardware.

2. Verilog

Verilog, short for "Verification Logic," is a hardware description language (HDL) that provides a means to model and simulate digital systems. Originally developed by Gateway Design Automation in the early 1980s, Verilog has become one of the most widely used HDLs in the semiconductor and electronic design automation industries [5]. Its popularity stems from its simplicity, readability, and powerful features, which facilitate the design, simulation, and synthesis of complex digital circuits.

At its core, Verilog allows designers to describe the behaviour and structure of digital systems using a syntax similar to traditional programming languages such as C and Pascal. Verilog modules, the building blocks of Verilog designs, encapsulate functional units of hardware and facilitate modular design practices. Modules can be instantiated, connected, and reused within larger designs, promoting scalability and reusability. Verilog's event-driven simulation model enables designers to model the dynamic behaviour of digital systems, simulating the propagation of signals through logic gates and registers over time. This simulation capability allows designers to verify the correctness and functionality of their designs before physical implementation, reducing time-to-market and mitigating costly design errors.

In addition to simulation, Verilog supports synthesis, the process of translating a high-level hardware description into a lower-level representation suitable for implementation on programmable logic devices such as field-programmable gate arrays (FPGAs) [6]. Synthesis tools analyze Verilog code and map it to the resources available on the target FPGA, optimizing for performance, area, and power consumption. The versatility of Verilog makes it well-suited for a wide range of applications, including digital system design, verification, and synthesis. Its ability to describe both behavior and structure at various levels of abstraction makes it an indispensable tool for hardware designers and engineers.

In the context of this thesis, Verilog serves as the foundation for implementing the Pac-Man game on the Spartan 3E FPGA platform. By leveraging Verilog's expressive syntax and simulation capabilities, this paper can translate the game's logic and graphics into hardware primitives, creating a faithful representation of the original gameplay experience.

3. Pac-Man game design and rule

Pac-Man, introduced by Namco in 1980, is a classic arcade game that revolutionized the gaming industry with its innovative gameplay mechanics and distinctive characters [7]. The game is set in a maze-like environment, where players control the eponymous Pac-Man character with the objective of navigating through the maze while consuming pellets and avoiding ghost enemies.

The maze consists of interconnected corridors and chambers, with pellets scattered throughout. As Pac-Man traverses the maze, he must consume all the pellets to advance to the next level. Additionally, four ghost enemies—Blinky, Pinky, Inky, and Clyde—roam the maze, seeking to thwart Pac-Man's progress. If a ghost catches Pac-Man, he loses a life. However, Pac-Man can turn the tables by consuming power pellets, temporarily granting him the ability to eat ghosts and earn bonus points. The behaviour of the ghosts adds an element of strategy to the game. Each ghost has its own distinct

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personality and movement pattern, making them unpredictable adversaries. Blinky, the red ghost, relentlessly pursues Pac-Man, while Pinky, the pink ghost, tends to ambush him from the sides. Inky and Clyde exhibit more erratic behavior, often alternating between chasing and retreating.

As players progress through the game, the maze layout becomes increasingly complex, with additional obstacles and power-ups introduced to challenge their skills. Bonus fruits periodically appear in the maze, offering additional points when consumed. The game continues until Pac-Man loses all of his life or completes all the levels, with players striving to achieve the highest score possible. The simplicity and addictive nature of Pac-Man's gameplay have cemented its status as a timeless classic, inspiring numerous sequels, spin-offs, and adaptations across various platforms and media.

In adapting Pac-Man for implementation on the Spartan 3E FPGA platform, the coding aims to preserve the core gameplay mechanics and rules while leveraging Verilog to realize the game's logic and graphical elements in hardware. By faithfully recreating the Pac-Man experience on FPGA, this paper hopes to showcase the versatility of hardware programming in replicating iconic gaming experiences.

4. Coding

This study will discuss the rotation direction of the pac man, then we will set the randomness of the obstacles, followed by the debounce and control buttons. Lastly, we will display the game and also the score count at the end of the game in VGA display with RGB component.

The implementation of the Pac-Man game using Verilog on the Spartan 3E FPGA platform encompasses a diverse set of functionalities, including rotation direction, randomization, debounce, control button, display management, and score counting. Each of these aspects is crucial for creating a faithful and immersive gameplay experience.

Rotation direction control is facilitated by Verilog modules that interpret user input from control buttons connected to the FPGA board. These modules detect button presses and translate them into directional commands, allowing players to navigate Pac-Man through the maze. Debouncing techniques are employed to eliminate mechanical switch bounce, ensuring reliable and consistent input recognition.

Randomization plays a pivotal role in determining the movement patterns of ghost enemies, adding an element of unpredictability to their behavior. Verilog modules generate pseudo-random numbers using algorithms such as linear feedback shift registers (LFSRs) or xorshift, which are then utilized to determine the next move of each ghost character. By incorporating randomness into the game logic, ghost movements appear more natural and varied, enhancing the challenge for players.

Control buttons are utilized for various game actions, such as starting the game, pausing/resuming gameplay, and navigating menu screens. Verilog modules interpret button presses and trigger corresponding events or state transitions within the game logic. Debounce circuits ensure that button presses are registered accurately, preventing unintended inputs or glitches.

Display management involves generating video signals compatible with the display hardware of the Spartan 3E FPGA board. Verilog modules utilize techniques such as rasterization and sprite rendering to generate graphical representations of the game elements, including the maze layout, Pac-Man character, ghost enemies, and score display. By synchronizing the timing of video signals with the display refresh rate, smooth animation and flicker-free rendering are achieved.

Score counting is implemented using Verilog modules that track the player's progress and update the score accordingly. Points are awarded for actions such as consuming pellets, eating ghosts, and completing levels. Score values are displayed on the screen using seven-segment displays or other output devices, providing feedback to the player and enhancing the overall gaming experience.

The integration of these functionalities into the Verilog codebase enables the creation of a fully functional Pac-Man game on the Spartan 3E FPGA platform. By leveraging hardware programming techniques, developers can implement complex gaming mechanics and interactions, pushing the boundaries of traditional software-based gaming.

This assignment assigns the value of the score signal to the led signal. It implies that the led signal is being used to represent or display the calculated total score.

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In summary, the code calculates the total score by summing up individual scores and assigns this total score to a signal called led. The led signal may be used to drive LEDs or other indicators in a hardware design to display the computed score.

For display code, this code is part of a system that assigns colors to pixels based on the position and geometry of different shapes (rectangle, triangles, and circles) and the value of less number. The resulting colors are assigned to the R, G, and B components, which typically represent the red, green, and blue channels of a pixel in a graphical system.

5. Conclusion

In conclusion, the development of a Pac-Man game using Verilog on the Spartan 3E FPGA platform has yielded valuable insights into the intersection of game design principles and hardware programming methodologies. Through meticulous design and implementation, these coding have successfully recreated the iconic gameplay experience of Pac-Man in a hardware environment, showcasing the versatility and power of FPGA technology.

One of the key findings of this paper is the feasibility of leveraging Verilog for game development on FPGA platforms. By utilizing Verilog modules to represent various components of the Pac-Man game, including the maze, Pac-Man character, and ghost enemies, this paper has demonstrated the ability to translate complex gameplay mechanics into hardware primitives. This approach not only enables efficient utilization of FPGA resources but also offers a scalable framework for future game development endeavors.

However, this project is not without its limitations. One of the primary challenges encountered during the development process was optimizing resource usage and performance on the Spartan 3E FPGA board. Due to the limited hardware resources available, compromises had to be made in terms of graphical fidelity and gameplay complexity. Future iterations of the project could explore techniques for optimizing resource utilization and enhancing performance, potentially leveraging advanced FPGA architectures or hardware acceleration techniques.

Furthermore, while the implemented Pac-Man game faithfully replicates the core gameplay mechanics of the original arcade version, there is room for improvement in terms of additional features and enhancements. Future studies could explore incorporating new gameplay elements, level designs, and power-ups to enhance the overall gaming experience. Additionally, integrating real-time multiplayer capabilities or exploring the use of advanced graphical techniques could further enrich the gameplay and expand the scope of the project.

In terms of further studies, this project opens up avenues for exploration in the realm of FPGA-based game development and hardware-accelerated computing. Future research could focus on adapting other classic arcade games or exploring innovative game mechanics tailored for FPGA platforms. Additionally, investigating the potential applications of FPGA-based gaming in educational contexts or embedded systems could yield valuable insights into the broader implications of this technology.

Despite these limitations, the successful implementation of Pac-Man on the Spartan 3E FPGA platform represents a significant achievement in the field of hardware-based game development. While this project serves as a proof-of-concept, it also lays the groundwork for future advancements in FPGA-based gaming and hardware-accelerated computing.

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