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Optimizing delay and energy in 4-bit absolute-value detector circuits: A balancing act

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Abstract. This research focuses on optimizing the 4-bit "absolute-value detector" circuit. This paper firstly introduces the basic theory of the circuit as the foundation of the analysis. It contains the function, logic and the theories which are used in the design. Secondly, this paper optimizes the circuit from two perspective, which are the delay and the energy. This research aims to find the relation between these two factors. Furthermore, because the delay and the energy are both critical to the performance of the circuit, and the conditions that determine one of the two factors also affect the other, this research also attempts to find a balance point which can optimize them as much as possible. In the end, this paper summarizes the result about the optimization and analyses the deficiencies of the experiment methods. This paper also gives suggestions about the perspective that the further studies can focus on in order to optimize the 4-bit "absolute-value detector" in a deeper degree.

Keywords: "absolute-value detector", optimization, delay, energy

1. Introduction

With the progress of The Times and the development of technology, computer has already become an indispensable tool in modern life [1]. Comparing absolute values is one of the most important operations in computer work, this is because in today's 64-bit computer operating systems, any input is converted into a string of 64-bit code and the computer will make logical judgments based on the comparisons in order to output the result. The optimization for "absolute-value detector" circuit is critical because it is related to the performance of the computer closely.

This research is going to focus on the basis 4-bit "absolute-value detector" because it is the basic unit of the "absolute-value detector" with more bits. This research will optimize the 4-bit "absolute-value detector" circuit from two aspects, which are the circuit delay and the circuit energy. Hence, in this paper, the first part is the basic theory analysis of the circuit. It covers the purpose and the logic of the design. The second part is the optimization from delay aspect. The delay of the circuit is related to the speed of the computer [2]. The third part is the optimization from energy aspect. Computer will generate heat in the process of running, how to reduce the heat production is an important problem in integrated circuit design [3].

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2. Basic Theory Analysis of the Circuit

2.1. Circuit Function

The "absolute-value detector" circuit plays a crucial role in signal processing and control systems. Its primary function involves assessing the magnitude of an input number or signal, which it does by comparing this magnitude with a predetermined threshold value. The comparison process is straightforward yet essential: the circuit evaluates whether the absolute value of the input exceeds, meets, or falls below the threshold. Based on this evaluation, the output is generated, which effectively represents the result of the comparison. This output can be a binary signal indicating a simple "yes" or "no" in response to whether the input value surpasses the threshold, or it can be more complex, providing detailed information about how the input compares to the threshold. This makes the absolute-value detector circuit a vital component in various applications, such as in electronic devices where precise measurement and control of signal strengths are required, in safety mechanisms where threshold detection is critical, and in data processing systems where signal validation is necessary. Its ability to accurately and efficiently determine the relationship between an input signal and a set standard makes it indispensable in many technological and engineering contexts.

2.2. Circuit Design

The circuit structure is based on the circuit logic, and the circuit logic is related to the function that the circuit aims to implement. In order to reflect the process of circuit design better and introduce the fundamental logic of the design more clearly, this paper will introduce the circuit design from 2 levels. The first level is from circuit logic aspect, and the second level is from circuit construction aspect.

2.2.1. Circuit Logic. In this research, the input number is represented by a binary complement [4]. In the 4-bit "absolute-value detector", the input signal is always a 4-bit binary number, $X_3X_2X_1X_0$. The decimal representation of this number is:

$$-2^3 \cdot X_3 + 2^2 \cdot X_2 + 2^1 \cdot X_1 + 2^0 \cdot X_0 \tag{1}$$

Although the decimal value -8 can be represented in binary complement by:

$$-2^3 \times 1 + 2^2 \times 0 + 2^1 \times 0 + 2^0 \times 0 \tag{2}$$

which is when $X_3X_2X_1X_0$=1000, in this research, this case is been ignored, which means 1000 will never occur as an input. Hence, the range of values for the input number is [-7, 7], so that the range of the magnitude of the input number is [0, 7].

The function of this circuit design is centered around outputting a signal that denotes the result of a comparison. Specifically, the output emits a "1" (indicating a high logic level) when the input number's magnitude surpasses the predefined threshold. In contrast, if the input's magnitude is less than or equal to the threshold, the output reflects a "0" (signifying a low logic level).

Central to this process is a "comparator" circuit, which is tasked with contrasting the input value's magnitude against the threshold. Notably, while the input is a 4-bit binary figure, the comparator's design requires consideration of only three of these bits. This specification arises from the fact that the input's most significant bit serves as a sign indicator, which is subsequently removed by the "absolute value convertor" circuit that we will discuss shortly [5].

Given that the input number is encoded in 4-bit binary complement form, it can represent both positive and negative values. A positive input has its most significant bit set to 0, while a negative input has this bit set to 1. The role of an "absolute-value detector" in this context is to establish a comparison of the input number's magnitude with a set threshold value. Prior to this comparison, it's necessary to ascertain the input's absolute value, necessitating a specific circuit for this purpose.

This circuit comprises two key components. The first is a "negative number detector" that ascertains whether the input number is positive. If it is, the number proceeds directly to the comparator. If not, it is routed to the second component, an "absolute value convertor." This segment of the circuit transforms a negative number, represented in complement form, into its absolute value. This

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transformation involves inverting each bit of the number and then adding 1, preparing it for the subsequent comparison process.

The logic of the entire circuit is the sequential combination of the 2 logics above. The input signal will pass the "negative number detector and absolute value convertor" circuit at first and then enters the "comparator" circuit to compare with the threshold value. The complete logic is shown in figure 1 [6].

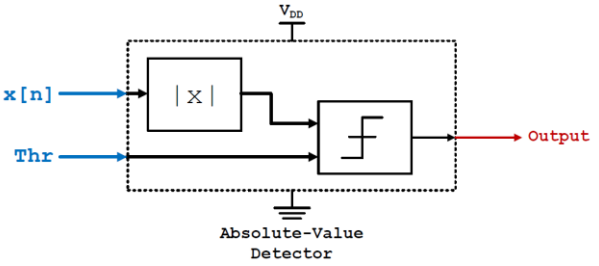

Figure 1. The complete logic [6]

2.2.2. Circuit Construction. In this research, the "negative number detector and absolute value convertor" circuit is going to be implemented by the design shown in figure 2.

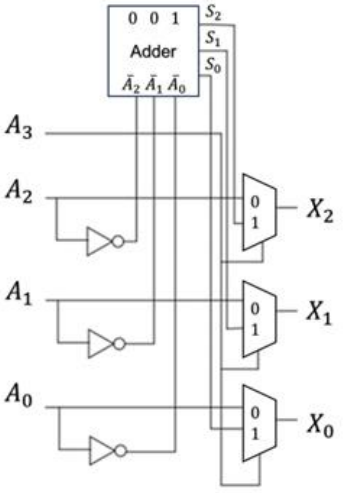

Figure 2. Negative number detector and absolute value convertor (Photo/Picture credit: Original)

This circuit contains 3 note gates, 3 MUXs and 1 adder. The construction of the adder is going to be introduced below. In this figure, A_3 is the most significant bit of the input number. If the value of A_3 is 0, which means the input number is positive, the MUX will send origin $A_2A_1A_0$ go to the comparator. And if the value of A_3 is 1, which means the input number is negative, the MUX will send the number which passes through the not gates and adder to the comparator, and this number is the absolute value of the negative number. The 3 not gates work to invert each bit of the input value, and the adder adds 1 to $\bar{A}_2\bar{A}_1\bar{A}_0$. This is the procedure mentioned earlier for getting the absolute value of a negative number.

As for the adder, the basic logic is shown in figure 3.

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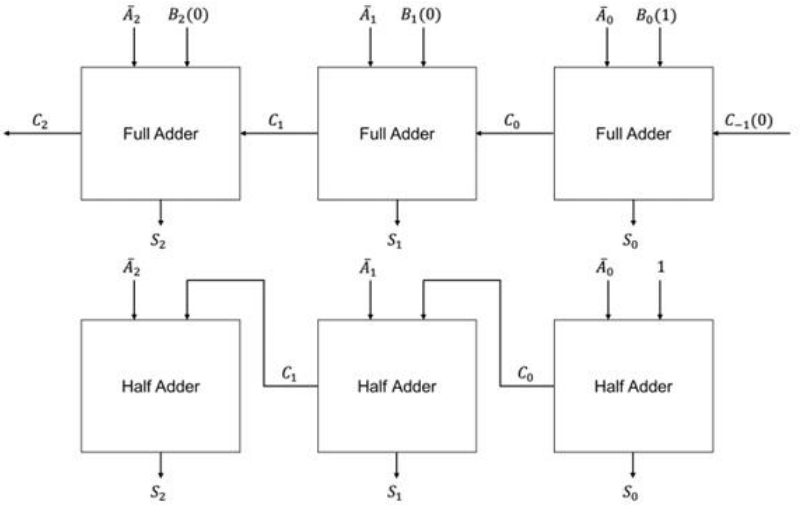

Figure 3. Adder basic logic (Photo/Picture credit: Original)

For each half adder, the value of A_i, C_i, C_{i-1} and S_i are shown in the truth table 1.

Table 1. Truth table

$A_i{}'$	C_{i-1}	C_i	S_i
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

According to analysis and simplification by K-map, the relation between C_i, $\bar{A}_i$, C_{i-1} and the relation between S_i, $\bar{A}_i$, C_{i-1} can be obtained, which are:

$$C_i = \bar{A}_i \cdot C_{i-1}$$

$$S_i = \bar{A}_i \oplus C_{i-1}$$

Consider each bit, the final simplified circuit of the adder is shown in figure 4.

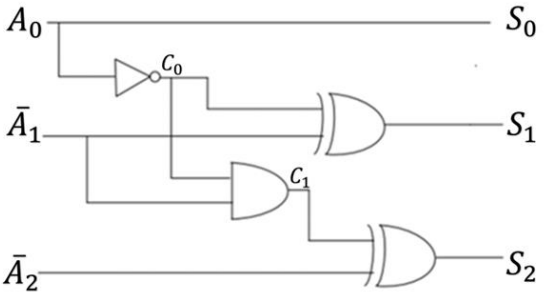

Figure 4. Simplified circuit of the adder (Photo/Picture credit: Original)

This research has designed 2 kinds of "comparators", which is shown in figure 5.

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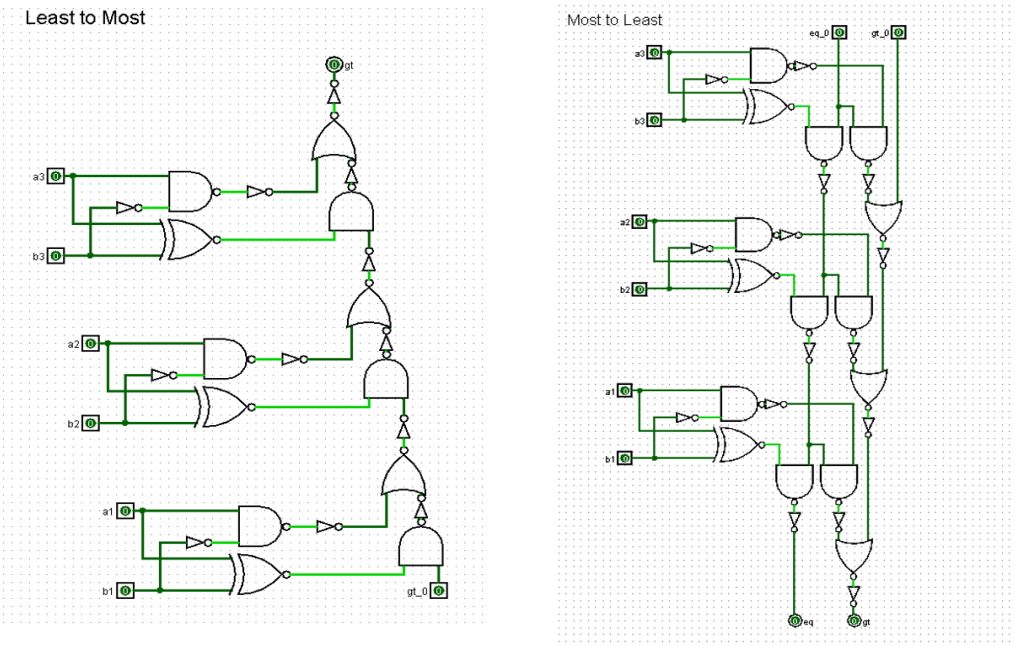

Figure 5. 2 kinds of “comparators” (Photo/Picture credit: Original)

There are two primary methods for comparing numbers in circuit design: one approach starts from the most significant bit and progresses towards the least significant bit, while the other method begins with the least significant bit and moves towards the most significant bit. Intuitively, the first approach might seem more efficient since, in cases where the most significant bit of one number is larger than that of the other, the comparison outcome can be immediately concluded, obviating the need for further bit-by-bit comparison.

However, in the realm of circuit design, designers must account for the worst-case scenario, where a conclusive result is only attainable after a complete comparison of all bits in both numbers. Therefore, when seeking an optimal design, factors other than initial intuition must be considered, with delay being a pivotal aspect.

This research has conducted a comparative analysis of the two design approaches from the standpoint of delay. It was found that the design which commences comparison from the least significant bit and progresses towards the most significant bit exhibits a reduced delay. As a result of this finding, this particular type of “comparator” has been chosen for implementation in the complete design, as depicted in figure 6. This choice prioritizes efficiency and speed, addressing the critical need for rapid processing in circuit operations.

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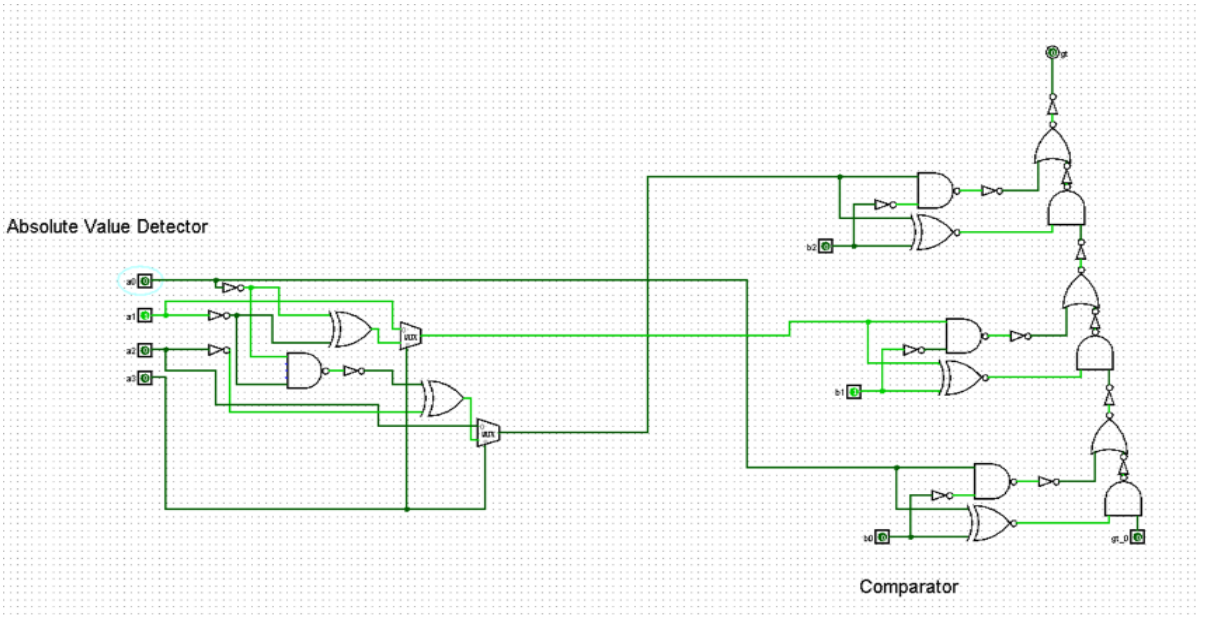

Figure 6. Complete design (Photo/Picture credit: Original)

3. Delay Optimization

This research applies Logical Effort Theory to analyze the delay of the circuit [7]. In order to simply the calculation, this research represent the delay of the whole circuit by the delay of the critical path of the circuit. The critical path of the circuit is shown in figure 7.

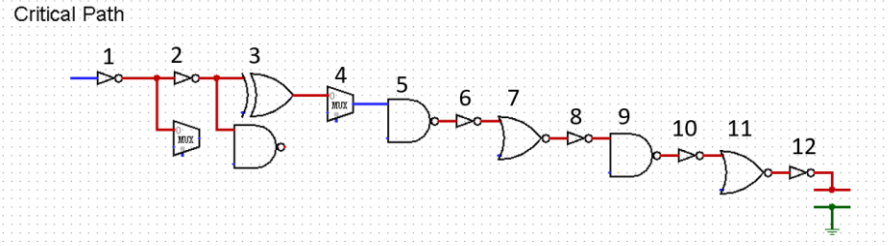

Figure 7. The critical path of the circuit (Photo/Picture credit: Original)

According to the calculation based on logic effort theory, the minimum delay of the circuit is 74.22 C units.

4. Energy Optimization

In this research, the maximum delay is set as 1.5 times the minimum delay. Here this research assumes that the size of every stage is the same, so that the whole energy is proportional to the energy of the critical path.

The formula for calculating the energy of the circuit is

$$E = \sum \alpha_i \cdot C_i \cdot {V_{dd}}^2 \tag{3}$$

Where α_i is the transition possibility of each stage, C_i is the logical size of each stage and V_{dd} is the source voltage [8].

According to the previous analyzation, the relation between the delay of the circuit and the energy of the circuit can be described as-A lower delay leads to a higher energy and a higher delay leads to a lower energy. Although the quantitative relation of them still needs more analysis to obtain. A good circuit design needs to consider both the delay and energy of the circuit, because a high delay will

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affect the function of the device, and a high energy will lead to a high heat power, which will bring more trouble to the heat dissipation of the device. Thus, the optimization scheme given in this study is to seek the lowest energy scheme under the maximum delay allowed.

In this study, the maximum allowable delay is set to 1.5 times the minimum delay, and this value is 111.33C unit. The gate size of each stage and the source voltage should satisfy follow formula [9].

$$\boldsymbol{Delay} = \sum \boldsymbol{g_i b_i h_i} + \sum \boldsymbol{p_i} \tag{4}$$

And in this case, this relation can be written as:

$$\boldsymbol{1.5 \cdot Delay_{min}} = [\boldsymbol{1 \cdot \frac{\frac{8}{3}+1}{1} \cdot \frac{C_1}{1} + 1 \cdot \frac{4+1.4}{4} \cdot \frac{C_2}{C_1} + 4 \cdot \frac{C_3}{C_2} + \frac{8}{3} \cdot \frac{C_4}{C_3} + 1.4 \cdot \frac{C_5}{C_4} + 1 \cdot \frac{C_6}{C_5} + 1.6 \cdot \frac{C_7}{C_6} + 1 \cdot \frac{C_8}{C_7} + 1.4 \cdot \frac{C_9}{C_8} + 1 \cdot \frac{C_{10}}{C_9} + 1.6 \cdot \frac{C_{10}}{C_{11}} + 1 \cdot \frac{32}{C_{11}} + 22}] \cdot \frac{V_{dd}}{(V_{dd}-0.2)^2} \tag{5}$$

Energy in this case can be written as:

$$\boldsymbol{E = V_{dd}^2 \cdot (C_1\alpha_1 + C_2\alpha_2 + C_3\alpha_3 + C_4\alpha_4 + C_5\alpha_5 + C_6\alpha_6 + C_7\alpha_7 + C_8\alpha_8 + C_9\alpha_9 + C_{10}\alpha_{10} + C_{11}\alpha_{11} + C_{12}\alpha_{12} + C_L\alpha_L)} \tag{6}$$

The value of each transition possibility in shown in table 2.

Table 2. The value of each transition possibility

α_1	α_2	α_3	α_4	α_5	α_6
$\frac{1}{4}$	$\frac{1}{4}$	$\frac{1}{4}$	$\frac{1}{4}$	0	0
α_7	α_8	α_9	α_{10}	α_{11}	α_{12}
$\frac{3}{16}$	$\frac{3}{16}$	$\frac{15}{64}$	$\frac{15}{64}$	$\frac{55}{256}$	$\frac{55}{256}$

To calculate the minimum energy under the limitation of the delay, the analyze with respect to each variable is needed. According to the energy formula, the energy can be considered as a function to 13 variables, which are V_{dd}, C_1, C_2, …, C_{12}. It can be expressed more clearly as:

$$E = f(V_{dd}, C_1, C_2, \ldots, C_{12}) \tag{7}$$

This research aims to obtain the relation of energy to V_{dd}. However, for each certain V_{dd}, the value of C_1, C_2, …, C_{12} will also influence the value of V_{dd}. Thus, the analysis to C_1, C_2, …, C_{12} is also needed to find the minimum energy under each V_{dd} [10].

From mathematic perspective, the method to achieve the analysis described above is to do partial derivative with respect to each C, and find the absolute minimum value when any other variables set a certain value. This process is complicated. This research uses computer program to complete this process.

The program contains 12 cycles. Because C_1 is a certain value 1 in the experiment circuit. The 12 cycles are the process to analyze the 12 other variables. The relation between E and V_{dd} is shown in table 3.

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Table 3. The relation between E and V_{dd}

V_{dd} (V)	E_{min} (C units)
0.775	NULL
0.795	NULL
0.815	5.916
0.835	5.926
0.855	6.018
0.875	6.188
0.895	6.369
0.915	6.595
0.935	6.829
0.955	7.070
0.975	7.323
0.995	7.627

It is worth noting that when V_{dd}=0.775V or 0.795V, the program cannot display the minimum energy correctly. This research proposes the following explanation for this phenomenon: This is because the energy optimization part of this research is based on the delay optimization part. According to the former theoretical analysis, in order to satisfy the maximum delay requirement, the minimum value of V_{dd} could be 0.775V. Precisely because of this, this research sets the V_{dd} region as [0.775V, 1V] in the energy optimization part. But in the program, during the loops executing, when the values of C_1, C_2, …, C_{12} change under each certain V_{dd}, they cannot change continuously. This means that each variable varies in units of a minimum step size. Otherwise, the program will have infinite calculations and it cannot be done. However, when the variables change under steps, the values of the delay cannot cover all the values in its range. And in this case, when V_{dd}=0.775V and 0.795V, the limitation that the delay equals to 1.5 times the minimum delay cannot be satisfied, so that the program reports an error.

The graph of E_{min} as a function to V_{dd} is obtained according to the result of the program is shown in figure 8.

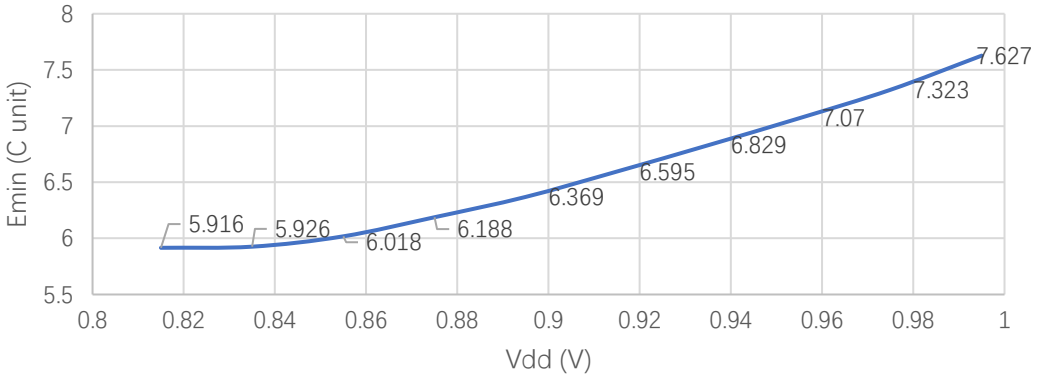

Figure 8. The graph of E_{min} as a function to V_{dd}

According to the trend of the function, this research chooses the energy when V_{dd}=0.815V as the optimal energy. Furthermore, the program also records the C values in this case, which are C_1=1(This is set up as an invariable value.), C_2=0.31, C_3=0.21, C_4=0.11, C_5=0.11, C_6=0.11, C_7=0.21, C_8=0.21, C_9=0.40, C_{10}=0.60, C_{11}=1.60, C_{12}=4.50.

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5. Conclusion

Based on the analysis and the experiment of this study, in conclusion, under the condition of circuit delay at 1.5 times the minimum delay, the minimum energy of the 4-bit "absolute value detector" circuit is 5.915V. This result basically meets with the expected result. However, there are still some parts in the experiment that can be improved to further improve the accuracy of the results.

Firstly, according to the energy optimization by the program, this research considers E_{min}=5.916C units as the best energy optimization. But when V_{dd}=0.775V and 0.795V, the program reports an error. Hence, it is also possible for the optimization to be at the points when V_{dd}=0.775V or 0.795V. The reason leads to this problem has already been discussed in the former part. The solution to this problem is to use computers with more computing power, thus reducing the number of steps the program runs in order to get the results closer to the real roots in mathematic.

Secondly, when the program analyses the influence of C values, although this research has set proper upper and lower bound for the C variables, the step lengths for running is too big, so that the C values obtained from the program can only reflect the approximate proportions between the values, but not the precise values. The first solution to this problem is also to use computers with more computing power to reduce the step lengths. And the second solution is to optimize the program with a better algorithm.

Moreover, this optimization did in this research aims to increase the performance of the circuit, and this mainly focuses on the circuit structure perspective and the control signal perspective. However, the most straightforward way to increase the circuit performance is to choose more efficient semiconductor devices, and the optimization from this aspect mainly based on the research on materials. Thus, the selection of higher quality semiconductor materials is also an important way to improve circuit performance.

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