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Design and hardware implementation of FIR digital filter

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Abstract. This article is about the hardware application of one of the basic filters (FIR filter) often used in digital signal processing. First, it introduces the development process of FIR digital filter and the development of FIR digital filter today, and then introduces FIR digital filter. The part combined with hardware, including the research on the hardware implementation technology of the programmable digital filter based on the emictor, the combination with the memistor and the combination with the programmable logic device FPGA is the second most typical research on the combination of digital signal processing technology and hardware in recent years, which respectively describes its main realisation. The combination of FIR digital filter and different hardware methods also has different advantages, but in general, compared with its separate development, the combination of hardware and it has more advantages.

Keywords: FPGA, hardware combination, memoresistor.

1. Introduction

With the gradual popularization of digitalisation and the increasing demand for digitisation and networking, and the more flexible digital signal processing system has become more popular. Gradually, digital signal processing technology has been widely used in various fields. Digital filter dominates the digital processing system, and its performance is related to the effect of digital processing. Digital signal processing technology can be applied in many fields, such as military, data communication, satellite and radar signal processing, audio signal processing, and so on. Digital filters play a crucial role in digital signal processing, as they can be used to extract useful signals from signals and remove interference signals. During the filtering process, some interference signals may not be completely removed, and some useful signals may also be damaged. Therefore, it is necessary to adjust and process the filtering results accordingly, ultimately obtaining the most ideal waveform possible [3]. Passive filters can cause significant pollution to the power grid [4].

The emergence of Fast Fourier Transform (FFT) algorithm in 1965 gave people a further understanding of the relationship between Finite Impulse Response (FIR) and Infinite Impulse Response (IIR)[5]. In the existing research, compared with one of the basic filters (IIR digital filter) often used in digital signal processing, FIR digital filter has many advantages such as linearity, stability and easy realization. Because of these advantages, FIR filter is easier in many engineering fields. With a wide range of applications, it can also create more value. It is found that there are still few processing methods and research results that combine FIR digital filters with hardware. Among them, the combination with memristors and programmable logic devices (FPGAs) is the second most typical research on the

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combination of digital signal processing technology and hardware in recent years [6]. This shows that the world has less research results and less application for the combination of FIR Filter and hardware. In view of the current situation, it is necessary to increase research on this aspect. Thus, the FIR digital filter and hardware can be integrated more effectively, so that it can improve Efficiency and bring benefits, thus facilitating people's lives and becoming more intelligent.

The first part of this article is the introduction. The middle of the period mainly includes the popularization of digitization, which is a more efficient technology for everyone to pursue, and the FIR digital filter is widely welcomed by everyone, b Ut there is very little research on it at present. The second part of this article mainly introduces the introduction of the combination of FIR digital Filter with three hardware and the basic principle of FIR digital filter, as well as its combinatio N with FPGA, verilogue and memory resistor and its principle. The third part of this article mainly shows that the combination of FIR digital filters and hardware Is achievable and has many benefits. It is necessary to continue to study the ways to combine them so as to help the development of FIR digital filters.

2. FIR digital filter based on hardware implementation

2.1. Introduction based on the hardware part

For the memory resistor, it actually represents the relationship between magnetic flux and charge. The research on the memory resistor is relatively complete. Memory devices are widely used in the field of chemistry and optoelectronics. It can also be applied to configurable switches, and its related characteristics can be applied to s Toring binary data. The memristor also has a typical application, time storage, and its memory resistance value is relate Ed to the net amount of current passing through it. There are two models of hardware circuits that can be adjusted for the memory resistor. By changing the voltage and current, this is a combination with the hardware [6]. They are the simplified memory resistor SPICE model based on the coupled variable resistance model, the memory resistor SPICE model based on the window function, and the memory resistor organisation resistance adjustment circuit based on switch control.

FPGA is an important module in programmable logic devices. FPGA uses a long hardware description language. It also uses the most commonly used hardware description language VHDL. FPGA is widely used in network and data processing, as well as instruments, military and other aspects of life. The part of the combination with hardware is the meaning, the optimisation and improvement of the variable programming logic hardware of the finite pulse response FIR digital filter.

2.2. Basic principle of FIR digital filter

The function of the filter is due to signal regulation, which is actually like a function of selecting and removing the signal frequency. FIR digital filter is a linear time-invariant system. It is a finite pulse response digital filter. It is composed of different lines, such as a series of linearly related delay circuits, each of which occupies a different time or weight. They can be used to realise the design of various filters, such as band-pass, band-through, low-pass, high-pass and other more complex filter design iii. There are also many advantages of using FIR digital filter, the most important of which is that it can achieve arbitrary frequency response. It not only has advantages but also disadvantages. For example, FIR digital filter requires a large number of delay circuits and more computing resources.

FIR digital filter system function:

$$\boldsymbol{H(z)}\overset{\boldsymbol{M1}}{\underset{\boldsymbol{n-1}}{==}}\boldsymbol{\sum h(n)z^{-n}}$$

Figure 1 shows the simplest filter by dividing the signal frequency - the low-pass filter:

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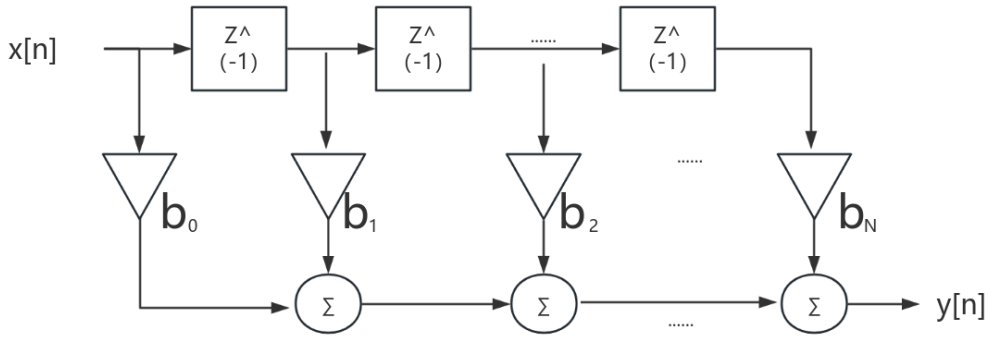

Figure 1. Low-pass filter structure diagram [6]

2.3. Combination of FPGA-based hardware and FIR digital filter

After using software to design the FIR digital filter, you can find the coefficient of the filter and its order. The subsequent method is to use FPGA to complete the hardware implementation part of the FIR digital filter.

The FIR digital filter directly constructs the FIR filter, which will take up a lot of resources, because it is mainly composed of multiplication units. The method of direct construction is super uneconomical and uneconomical. In some views, it is proposed to use FPGA hardware to realise the filter results. Figure 2 T of the filter OP-DOWN structure diagram [7].

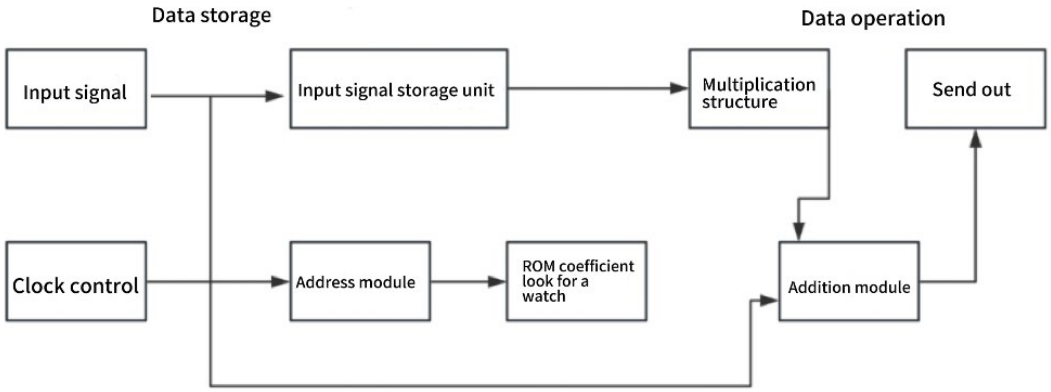

Figure 2. TOP-DOWN structure diagram of the filter [7]

The TOP-DOWN structure of the filter uses a serial structure to multiply the input data by the coefficient of its corresponding filter, but this operation is also different from the operation in the figure. This is the product lock in the previous level, and then directly do a cumulative operation with the product of the latter level, not all the numbers. After multiplying, do the accumulation. The above methods can save a lot of hardware resources, reduce costs, be more economical, and finally achieve a process of improving the speed of execution. The two modules (data storage and data operation) are the most important systems of FIR digital filters. The digital storage module uses the clock control plate to select the signal and decode the address, and read out the data corresponding to the ROM address in the ROM lookup table, which is the filter coefficient. Then they and its corresponding input signal are synchronously output to the data operation module. Its main function is to complete the input signal and the corresponding The multiplication and accumulation of the filter coefficient [7].

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The combination of FIR digital filter and FPGA mainly realises the saving of resources and economic costs.

2.4. Based on verilog VHDL realised through JTAG and using FIR digital filter

Use FPGA hardware to verify whether the conclusion of the implementation in the software part is correct. In some literature, after completing the software simulation, use vivado software to edit the verilog HDL program, and then combine with the FPGA hardware test platform to carry out actual engineering testing, and then control it through JTAG and The observation signal parameter setting is the same as the software simulation parameter. The parameter selection of the multi-functional filter is controlled by VIO, and then the signal is observed through ILA. Then carry out the filtering operation. Through the combination of the hardware and software of this FPGA and FIR digital filter, this engineering test verifies the optional variability of the parameters of the multi-functional FIR digital filter, which can adapt to various scenarios of different filter demand signals, with stronger flexibility, better real-time and more stability. Good, more practical.

2.5. FIR digital filter based on resistor

Based on the design of the FIR digital filter of the remistor, the basic circuit realisation of the programmable first type of linear FIR filter is first studied, and the cross-array structure of the mestor-based is realised to realise the weighting of these sampling and delayed signals, mainly using the even-symmetry of the coefficients of the first type of linear phase FIR digital filter. Mass, $0 \leqslant n \leqslant N-1$, there is always h(n)=h(N-1-n). Another structure is proposed. The filter coefficient of the FIR filter will reflect the magnification through the feedback resistance and memory resistor of the amplifier. Among them, the memory resistor can be changed in other ways. By adjusting the circuit, it is finally found that the FIR digital filter can be programmed [4].

Figure 3 shows the structure of the programmable digital filter.

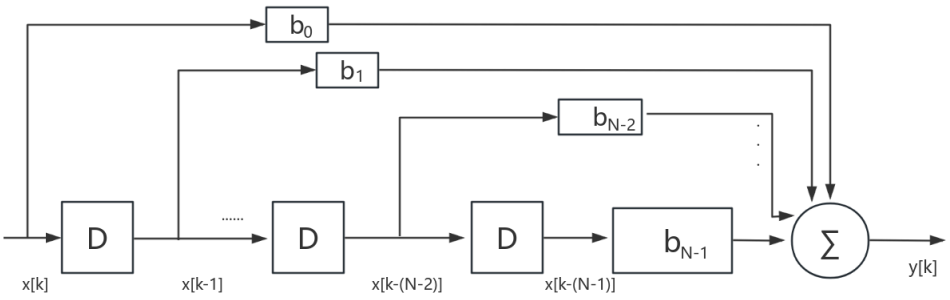

Figure 3. Programmable digital filter structure [6]

In the circuits designed with mestors, there are various circuits designed, such as the mestor model based on capacitance and controlled power supply, and the model of memistor based on window function control, etc. The resistance value of the memory resistor can be easily changed directly through the peripheral resistance adjustment circuit without replacing the hardware circuit, so the FIR digital filter is programmable [1]. The advantage of the memoristor is to use the multiplication method to complete the combined relationship between the memorator and the operational amplifier, which omits and avoids some more complex multiplication calculation processes. All calculations are carried out in parallel, so that it can be used to realise a high-order FIR digital filter. In this circuit, there is no need for modulus. For converters, such a design can further reduce and avoid some errors caused by quantisation. Generally speaking, the speed of filtering is not limited by the analogue-to-digital converter.

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Assuming that the resistance value Mk of all memory resistors has been adjusted to the desired resistance value and remains unchanged in the process of circuit operation, it can be seen from the nature of the "virtual break" and "virtual short" of the operational amplifier [6].

$$y[n]=\{\frac{x[n]}{M_0}+\frac{x[n-1]}{M_1}+\ldots+\frac{x[n-(N-1)]}{M_{N-1}}\}R_f$$
$$=-\frac{R_f}{M_0}x[n]-\frac{R_f}{M_1}x[n-1]-\frac{R_f}{M_2}x[n-2]-\ldots-\frac{R_f}{M_{N-1}} \quad (2\text{-}1)$$

The corresponding relationship between the filter coefficient and the resistor value of this circuit can be obtained:

$$b_0=-\frac{R_f}{M_0},\ b1=-\frac{R_f}{M_1},\ b2=-\frac{R_f}{M_2},\ \cdots,\ b_{N-1}=-\frac{R_f}{M_{N-1}} \quad (2\text{-}2)$$

From the formula (2-2), it can be seen that the basic circuit of the first type of programmable linear phase FIR filter is negative. The coefficient of the FIR filter is expressed as the ratio of the feedback resistance Rf of the amplifier to the resistance of the branch memory resistor Mk. For filters with all negative coefficients, through Rj and memory resistors M0, M1, M2... The resistance increase value of MN can be appropriately selected and adjusted to make the ratio consistent with the coefficient of the first type of linear phase FIR digital filter. For the ratio of all positive coefficients. It can be done by adding an inverse proportional amplifier to the end of the filter circuit.

3. Conclusion

FIR (limited impact response) digital filter has been widely used in hardware implementation because of its simple structure, good stability and easy implementation. In the hardware implementation, the FIR filter can adopt a variety of structures, such as direct type, cascade type, frequency sampling type and fast convolution type, etc [8-9].

Among them, direct structure is the most commonly used, especially when FPGA is implemented, different structural designs such as serial structure or parallel structure can be adopted.

In the process of hardware implementation, the determination and quantification of filter coefficients are the key steps. You can use MATLAB and other software tools to simulate the filter design code and quantify the filter parameter coefficient. There are many ways to quantify the coefficient, which can be implemented by using the function in MATLAB, or using the relevant filter design software tool to customise the window function filter coefficient to meet the current needs.

At present, there are still few realisations of this theme at home and abroad. However, through investigation, it can be seen that the combination of FIR digital filter and hardware still has many advantages. It can not only save resources and economic costs, but also verify the optional variability of the parameters of the multi-functional FIR digital filter. It can adapt to various scenarios of different filter demand signals, with stronger flexibility, better real-time, better stability and higher practicality. It can also reduce errors and speed up some processing. Moreover, the current FPGA has many advantages. For example, it has higher practicality, smaller area, more exquisite and more reliable. This is a hardware solution that may be used frequently in the hardware realisation of digital filters.

To sum up, the conclusion of the combination of FIR digital filter and hardware is that through reasonable design and implementation strategy, the advantages of FIR filter can be given full play to achieve efficient and stable digital signal processing. In practical application, it is necessary to choose the appropriate structure and implementation method according to the specific performance requirements and resource limitations to achieve the best performance and resource utilisation. In summary, the combination of FIR digital filters and hardware provides a new approach for the development of filters [10].

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References

[1] Guo Guanghao, Liu Zhizhe, Meng Qinglong, etc Design and verification of multi-level parallel pipelined FIR digital filters [J] Modern Electronic Technology, 2015, 38 (1): 69-72
[2] Li Yong, Liu Wenyi Design of a high-speed image data acquisition and storage system [J] Computer Measurement and Control, 2013,21 (2)
[3] Zhang Zhen, Research on FIR Digital Filters Based on FPGA [J] School of Computer Science, 2016,12 (4)
[4] Wang Zhichao. Low pass filter based on FPGA [D]. Harbin Institute of Technology, May 2012
[5] Yang Sujun. Research on Structural Vibration Detection System and Vibration Mode Testing Method [D], 2003
[6] Research on hardware implementation technology of programmable digital filter based on memory resistor. Geng Hao.2017 CNKI
[7] Realise the hardware system design of FIR digital filter based on FPGA devices. Xu Yan, Sun Lihua.2020.7.22. Microcomputer information
[8] Optimised design and hardware implementation of FIR filter Wang Jinming, Zhang Xiongwei - TV Technology - 2003.03.17
[9] Comprehensive experimental design of software and hardware combined with Matlab and FPGA Shi Haoqiang; Jiang Zhanjun; - Laboratory Research and Exploration - 2020.01.25
[10] Zhao An, Yan Yihua, Chen Linjie, Liu Donghao, Wang Wei, Chen Zhijun, Improvement method of high-speed FIR digital filter design based on FPGA, Key Laboratory of Solar Activity of National Astronomical Observatory, Chinese Academy of Sciences, December 2015 (01)