# A review of physical heat dissipation methods for 3D integrated technology

#### Chengxuan Li

Zhongkai University of Agriculture and Engineering, Guangzhou, Guangdong, 510550, China

#### p77979196@126.com

Abstract. Three-dimensional integrated circuits have higher integration than two-dimensional integrated circuits, and can obtain higher performance and lower power consumption in a certain space. In order to fulfill higher efficiency, thermal management becomes particularly important in 3D integration technology. However, the traditional heat dissipation method cannot satisfy the heat dissipation needs of three-dimensional integrated circuits, which require better heat dissipation methods to be developed. This paper introduces the realization of three-dimensional integrated circuit using silicon via (TSV) technology, which allows the chip to be vertically stacked to transmit information. This paper summarizes the research methods and findings of three-dimensional integrated circuit heat dissipation in recent years, including thermal through silicon via (TTSV) and microchannel cooling. It also emphasizes the advantages and disadvantages of both mehods, and the challenges faced in current research via an overview. The future research trend for both heat dissipation methods mainly consists of combining special algorithms to achieve thermal-electrical codesign and thermal management of three-dimensional integrated circuits.

**Keywords:** three-dimensional integrated circuit, through silicon via, thermal through silicon via, microfluidics cooling.

#### 1. Introduction

Moore's observation and summary in 1965 showed that the number of transistors that can be accommodated on an integrated circuit doubles every 18 to 24 months, with a corresponding decline in cost. The introduction of Moore's Law has promoted the development of integrated circuits in the past 40 years, and has also made integrated circuits popular in various electronic devices. However, due to the failure of Moore's Law, the traditional 2D IC technology has reached a bottleneck [1]. Three-dimensional integrated circuit (3D IC) technology will become the research focus of chip development in the post-Moore era.

The realization of 3D IC extends Moore's law to another dimension by implementing TSV technology, which enables information transmission in the vertical direction of the chip, thus making 3D IC technology possible. In terms of performance, the vertical stacking of chips allows 3D integrated circuits to handle more work than 2D integrated circuits. In terms of power consumption, due to the shortening of the line length, the path of information transmission is reduced, and the power consumption is reduced. In terms of integration degree, the stacking of wafers increases the density of

<sup>© 2024</sup> The Authors. This is an open access article distributed under the terms of the Creative Commons Attribution License 4.0 (https://creativecommons.org/licenses/by/4.0/).

wafers, improves the integration of devices, and reduces the volume and weight of devices. However, high-density chip stacking generates a lot of heat, so heat dissipation is one of the main problems facing 3D IC at present. In order to popularize this technology in a large area in various industries, it is necessary to find an effective way to solve the heat dissipation of 3D IC. The thermal management of 3D IC is achieved through the physical heat dissipation of material, structure, and process [2-4]. The other is to compose architecture-level heat dissipation through thermal modeling and special algorithms to achieve thermal-electrical codesign and thermal management of 3D IC [5]. At present, most people's research method is to find the best and most effective algorithm model through thermal modeling, while there is a lack of research on physical heat dissipation. Therefore, this paper studies the influence of different materials and process technologies on the heat dissipation of 3D IC in physical heat dissipation, including TTSV insertion and microfluidic cooling. Since the combination of physical heat dissipation algorithm models is the primary trend in the future, the compilation of related information in this paper can provide information to inform and assist related researchers.

## 2. TSV technology

## 2.1. TSV production process

Since the signal processing between chips in 3D IC is vertical, different from the horizontal transmission in 2D IC, a new way to realize 3D IC is needed. At present, the main research directions are based on TSV, through etching holes on the chip, and then through filling materials to become the channel of signal vertical transmission. The process of TSV mainly includes etching holes, the filling of holes and electroplating[6].

The process of etching holes started with etching on the silicon wafer using an etching agent, and after producing a passivation film, deeper etching is produced by bombardment, and finally the passivation layer is cleaned. The holes created by the etching form channels that allow the multilayer wafers to transmit signals while stacked vertically.

Hole filling uses metal as a filler material, a dielectric layer is essential to electrically isolate the holes from the silicon substrate. The usual filling methods include physical vapor precipitation and chemical vapor precipitation, among which PECVD and SACVD are the main methods for chemical vapor precipitation. After the deposition of the dielectric layer is the barrier layer, which prevents the diffusion of Cu atoms.

The advantage of conformal copper plating is that the process is simple, the disadvantage is the discontinuity of the Cu seeds and the limitation of equipment application. However, the advantage of the bottom-up plating process is that it ensures the integrity of the filling without gaps. The advantage of super conformal packing is that there is no size limitation. Due to the superior conductivity and compatibility of Cu materials with CMOS processes, TSV conductive filling is currently generally achieved by copper plating. The goals of electroplating are low stress, no holes, and no voids during the manufacturing [7].

# 2.2. Heat dissipation capacity of TSV

In the production process of TSV, special materials can be used, and different structural layouts in the chip can change the heat dissipation capacity of the TSV in the 3D IC. However, in terms of thermal conductivity, there is another metal filling material, carbon nanotubes (CNT), which can have better thermal conductivity on TSV and better heat dissipation performance on 3D IC compared with the current mainstream metal copper material. At the same time, TSV not only has different thermal characteristics in the selection of filling materials, but will also be affected to a certain extent. In other aspects, the shape, structure, layout, and the density of insertion of TSV will affect its thermal characteristics [8].

Although TSV plays a great role in the realization of three-dimensional integration technology, the silicon through hole in the chip provides a good idea for the horizontal transmission of traditional 2D IC to the vertical transmission of 3D IC, but the heat dissipation problem of vertical stack is one of the

main challenges of 3D IC, so the study of the thermal characteristics of TSV appears to be important. Strengthening the thermal conductivity of the TSV can reduce the heat dissipation pressure of the 3D IC to a certain extent.

# 3. Insert TTSV

Due to the superposition of multiple chips, the workload of 3D IC increases exponentially compared with that of 2D IC. The high degree of concentrated completion makes the heat of 3D IC exponentially larger than that of traditional 2D IC. Although metal cu, the mainstream filling material for TSV, has much better thermal conductivity than silicon, it still cannot meet the heat dissipation capacity required for 3D IC work. Therefore, the ordinary TSV is improved into a TTSV designed for heat dissipation. Inserting TTSV into the wafer is the simplest and most effective method to solve the heat dissipation problem of 3D IC. TTSV is a kind of TSV, but it cannot transfer signals between vertical chips and can only be used for 3D IC heat dissipation. The role of TTSV is mainly heat transfer, transferring heat from a high temperature area to a low temperature area, or transferring heat from a high temperature chip to another chip with a lower temperature, preventing the heat concentration of the 3D IC in the work. Since the heat in the 3D IC is mainly in PDL, TTSV is to be placed in PDL. The hotspots can be expanded to reduce the power consumption density, thereby reducing the heat density, and the TTSV can be inserted in its center to reduce the temperature of the hotspots, thereby reducing the temperature of the layers. However, inserting TTSV into the center of the chip assumes that the heat of the chip is concentrated in the central position as a prerequisite. In reality, the heat distribution of the chip is uneven, so TTSV cannot be inserted into the central position ideally, and the heat distribution of the chip must be obtained through a special algorithm. In this way, the best TTSV distribution position can be obtained, so that the thermal conductivity of TTSV can be maximized, and the heat dissipation problem of 3D IC can be effectively solved [9]. In order to ensure the reliability of TSV operation, the number of TSV should be limited, resulting in the number of TTSV should also be limited, and TTSV can only be inserted in the position where heat dissipation is most needed, that is, the area with the highest heat density [10]. The thermal conductivity of TTSV is affected not only by the location distribution of TTSV in the chip, but also by the filling material of TTSV and the structure of TTSV. At present, the main filling material of TTSV is metal copper. However, compared with metal CNT, metal CNT not only has better cooling ability on TSV, but also can make the heat dissipation effect of TTSV more obvious as the filling material of TTSV [11]. In terms of the structure of TTSV, the TTSV with significant cooling ability at present is the TTSV with fin-shaped geometry [12]. Compared with the ordinary TTSV, its advantage on the single layer is that it can cool the water away from the TTSV, so that the cooling range of TTSV is extended to a certain extent, because it is not limited by the specific location. The original number of TTSV can be reduced again, so that the reliability of TTSV can be improved. However, the thermal conductivity of TTSV with fin geometry on multi-layer TTSV and single-layer TTSV is somewhat different, and the research on the heat dissipation capacity of TTSV on multi-layer TTSV needs to be further discussed [13].

# 4. Microfluidic cooling technology

Microfluidic cooling technology is the main research direction for 3D IC heat dissipation at present. Since the specific heat capacity and thermal conductivity of liquids are both higher than those of air, traditional air heat dissipation cannot solve the huge heat of 3D IC. Therefore, microfluidic cooling technology is a good method to optimize the heat dissipation of 3D IC.

Because the number of TTSV is limited by the number of overall TSVS, there is always a module area far away from TTSV in each layer of the chip, and the heat generated by its work is difficult to transfer to other layers of the chip. Therefore, etching microfluidic on the back of the chip can cover the whole chip better than inserting TTSV. The heat generated by the modules in each area is taken away by the coolant, thereby reducing the temperature of each layer of the chip, which is a good solution to the heat dissipation problem of the 3D IC. To exert the cooling ability of microfluidic, it is necessary to study the thermal resistance of microfluidic. The thermal resistance of the microfluidic radiator and the

size of the wafer, the thermal conductivity of the wafer substrate, the flow rate of the coolant, the thermal properties of the coolant, the number of microfluidic, the width of the microfluidic, the height of the microfluidic and the distance between the bottom surface of the microfluidic and the device layer, and other joint decision [9]. At the same time, the correlation between the heat dissipation capacity of the microfluidic and the density and electrical performance of the electrical TSV. The diameter and depthwidth ratio of TSV can be well controlled to maximize the heat dissipation capacity of microfluidic [14]. However, non-uniform heating of the chip is also the main challenge of microfluidic cooling. If there is no method to accurately determine the location of the hotspots, the hotspots can only be observed through a digital system. In addition, parameters in microfluidic are changed in real time to achieve the best effect of microfluidic cooling, or build a model to predict hotspots [15-16]. The insertion of TTSV and microfluidic cooling can be combined, which is also the research direction to solve the heat dissipation problem of 3D IC, and can maximally reduce the temperature of 3D IC during operation [17]. The proposed hybrid cooling scheme provides much better cooling capability than using only thermal TSVs, although it consumes 56% less cooling power compared with pure micro-channel cooling [18].

## 5. Conclusions

With the advent of the post-Moore era, the development of 2D IC has ushered in a bottleneck period. The development of 3D IC is very promising at present, and the main challenge of 3D IC is the problem of heat dissipation. This paper introduces the realization of 3D IC by TSV, and the factors affecting the thermal conductivity of TSV in the TSV process. At the same time, the main methods to solve the heat dissipation problem of 3D IC are summarized: TTSV insertion and microfluidic cooling. Moreover, the advantages and disadvantages of TTSV and microfluidic cooling are introduced, and the current research directions on optimizing the heat dissipation abilities of them are also introduced. At present, the main challenge between the two is that the specific location of hotspots cannot be determined. If a method can be found to evaluate the location of hotspots, that is, it is necessary to combine the architecture level thermal modeling algorithm and thermal modeling to make a great breakthrough in the heat dissipation problem of 3D IC. The heat dissipation of 3D IC cannot be studied only at the physical level. Only by solving the heat dissipation problem of 3D IC is it possible to develop 3D IC technology and thus improve chip performance.

However, this paper only analyzes and summarizes the current mainstream 3D IC thermal management research, and does not do experimental analysis. Moreover, only two physical heat dissipation methods of 3D IC are introduced. Based on the above shortcomings, other heat dissipation methods will be added in the future, and these methods will be analyzed through experiments, and the effectiveness of various heat dissipation methods will be proved according to the experimental results.

## References

- [1] Theis T N, Wong H S P. The end of moore's law: A new beginning for information technology[J]. Computing in science & engineering, 2017, 19(2): 41-50.
- [2] Chen K N, Tu K N. Materials challenges in three-dimensional integrated circuits[J]. Mrs Bulletin, 2015, 40(3): 219-222.
- [3] Tavakkoli F, Ebrahimi S, Wang S, et al. Thermophysical and geometrical effects on the thermal performance and optimization of a three-dimensional integrated circuit[J]. Journal of Heat Transfer, 2016, 138(8): 082101.
- [4] Topol A W, La Tulipe D C, Shi L, et al. Three-dimensional integrated circuits[J]. IBM Journal of Research and Development, 2006, 50(4.5): 491-506.
- [5] Salvi S S, Jain A. A review of recent research on heat transfer in three-dimensional integrated circuits (3-D ICs)[J]. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2021, 11(5): 802-821.
- [6] Shen W W, Chen K N. Three-dimensional integrated circuit (3D IC) key technology: Throughsilicon via (TSV)[J]. Nanoscale research letters, 2017, 12: 1-9.

- [7] Wang X, Chen D, Li D, et al. The development and progress of multi-physics simulation design for TSV-based 3D integrated system[J]. Symmetry, 2023, 15(2): 418.
- [8] YANG Zhiqing, PAN Zhongliang. Research on Thermal Characteristics of TSV in 3D Integrated Circuits[J] (in Chinese). Semiconductor Optoelectronics, 2019, 40(06): 820-825.DOI:10.16818/j. issn1001-5868.2019.06.015.
- [9] Feng D A I, Zhong-Liang P A N. OPTIMIZED METHOD FOR THERMAL THROUGH SILICON VIA PLACEMENT WITH NON-UNIFORM HEAT SOURCES IN 3-D-IC[J]. Thermal Science, 2023, 27.
- [10] Yang GuoBing. Research on Thermal Optimization of Three-Dimensional Integrated Circuit Based on Area Extending and Thermal Through Silicon Vias[D] (in Chinese). Hefei University of Technology, 2014.
- [11] Cui YuQiang, Pan ZhongLiang. Heat dissipation performance of TTSV in 3D integrated circuits[J] (in Chinese). Electronic Technology & Software Engineering, 2018, (18): 81-83.
- [12] Hwang L, Lin K L, Wong M D F. Thermal via structural design in three-dimensional integrated circuits[C]//Thirteenth International Symposium on Quality Electronic Design (ISQED). IEEE, 2012: 103-108.
- [13] Huang L J, Zhao W S. Thermo-mechanical analysis of an improved thermal through silicon via (TTSV) structure[J]. Progress In Electromagnetics Research M, 2013, 30: 51-66.
- [14] Li Xiuhui. Thermal Management Research of Three-Dimensional Integrated Circuit with Micro-Channels[D] (in Chinese). XIDIAN UNIVERSITY, 2018.
- [15] Wang S, Yin Y, Hu C, et al. 3D integrated circuit cooling with microfluidics[J]. Micromachines, 2018, 9(6): 287.
- [16] Wang K J, Sun H C, Pan Z L. An analytical thermal model for three-dimensional integrated circuits with integrated micro-channel cooling[J]. Thermal Science, 2017, 21(4): 1601-1606.
- [17] Wang K J, Sun H C, Li C L, et al. Thermal management of the hotspots in 3-D integrated circuits[J]. Thermal Science, 2018, 22(4): 1685-1690.
- [18] Shi B, Srivastava A, Bar-Cohen A. Co-design of micro-fluidic heat sink and thermal throughsilicon-vias for cooling of three-dimensional integrated circuit[J]. IET Circuits, Devices & Systems, 2013, 7(5): 223-231.