Proceedings of the 2nd International Conference on Functional Materials and Civil Engineering
DOI: 10.54254/2755-2721/89/20241075

Research on the design and application of Analog-to-Digital converters

Ruxin Zhang

Aerospace Engineering, Carleton University, 1125 Colonel By Dr, Ottawa, Ontario K1S 5B6, Canada

1141637042@qq.com

Abstract. In the modern digital era, the conversion of analog signals to digital data is a crucial process for a wide range of applications in industries such as consumer electronics, medical devices, and telecommunications. The accelerated evolution of digital technology is driving a surge in demand for high-performance analog-to-digital converters (ADCs). The paper presents a comprehensive analysis of analog-to-digital converters, emphasizing their types, applications, performance measurements, and most recent developments. In the paper, emphasis is placed on the mechanisms of different ADC architectures, such as Successive Approximation Register (SAR), Sigma-Delta (Σ-Δ), and Flash ADCs, and their respective strengths and weaknesses are evaluated. In terms of technique, it synthesizes and summarizes research results from multiple academic sources and technical papers. In addition to underscoring the pivotal concerns of ADC design, including power consumption, resolution, and sample rate, the research delves into novel approaches that leverage the use of advanced materials and techniques. The research results demonstrate the continued development of ADC technology and its critical function in improving the effectiveness and performance of digital systems.

Keywords: Analog-to-Digital Converter (ADC), Signal Processing, SAR ADC, Sigma-Delta ADC, Flash ADC.

1. Introduction

Modern digital systems require the conversion of analog signals into digital format in order to function, where ADCs serve as the link between the analog and digital domains to convert continuous signals accurately and efficiently. ADCs are used in a multitude of applications, such as consumer electronics, automotive systems, medical equipment, and telecommunications. The field of ADC technology has witnessed significant advancements in the last few decades, driven by the growing demand for reduced power consumption, enhanced sampling rates, and higher resolution. And SAR ADCs employ a binary search method to convert analog input signals to digital outputs, where comparators, successive approximation registers, sample and hold circuits, and DACs are the main components. It is suitable for battery-powered portable devices due to its low power consumption advantage, which allows a fair trade-off between speed and resolution. Moreover, its simple architecture reduces cost and simplifies deployment. This paper aims to provide an in-depth review of ADCs, including the latest technological developments, classification of various ADC types, basic operating principles, and performance evaluation criteria. To this end, an attempt has been made to provide an in-depth insight into the current

© 2024 The Authors. This is an open access article distributed under the terms of the Creative Commons Attribution License 4.0 (https://creativecommons.org/licenses/by/4.0/).

DOI: 10.54254/2755-2721/89/20241075

status and future trends in ADC technology, highlighting the challenges and potential solutions in this area.

2. Fundamental Theory and Key Technologies of ADCs

The Nyquist-Shannon Sampling Theorem, which states that a continuous signal can be completely reconstructed if it is sampled at a rate greater than twice its highest frequency, serves as the foundation for digital signal processing. And Kotelnikov's theorem represents a foundational principle in the development of digital control systems (DCS).

The Kotelnikov-Shannon Theorem elucidates, through Kotelnikov and Shannon's formulation, that samples taken at intervals of $1/2f_c$ seconds can completely characterize a signal with a maximum frequency of f_c, provided that the signal's frequency is not higher than f_c [1]. The process of transferring a greater amount of input values to a smaller set of input values, such as rounding the input values to a predetermined number of levels, is called quantization and encoding. At this stage, quantization error is introduced, playing a critical role in determining ADC performance. In contrast to conventional quantization techniques that rely on digitally valid comparator outputs, which are subject to lengthy regeneration periods and impose constraints on ADC speed, metastability zone-based quantization employs metastability zones to circumvent these limitations. This markedly reduces the time required for comparator regeneration, thereby enhancing the speed of the ADC [2].

3. Design and Application of Various ADCs

There are many ADC designs available, such as SARs, Sigma-Delta, and Flash ADCs, each with a different principle of operation and advantages and disadvantages.

3.1. Successive Approximation Register (SAR) ADC

The low-power design architecture of the SAR features a structure comprising a sample-and-hold, a comparator, a SAR, and a digital-to-analog converter (DAC) [3]. It converts continuous analog input signals into digital representations by means of a binary search algorithm. The SAR is initialized with the Most Significant Bit (MSB) set to the digital value '1' and the remaining bits set to zero at the start of the operation. The comparator compares the analog value that corresponds to the digital code fed to the DAC with the sampled input [3]. The comparator resets the MSB to '0' if the DAC output is higher than the sampled input; otherwise, it remains at '1'. This binary search continues for all bits in the SAR [3].

In addition, the 65 nm CMOS 10-bit 50-MS/s asynchronous SAR ADC contains the comparator, a charge redistribution DAC, a bootstrapped switch, and successive approximation control logic [4]. A dynamic comparator with a preamplifier and latch structure is employed in the design to boost the conversion speed and diminish the power consumption. The capacitor array uses a fully differential structure to suppress interference and even harmonics [4]. To minimize charge/discharge time and power consumption, the first three bits of the DAC capacitor array are divided and switched using a split-monotone switching strategy, while the rest of the capacitors switch using a monotone switching technique. Without the need for a high-frequency clock, asynchronous logic is capable of generating high-frequency control signals that correspond to circuit conversion [4].

This low-power design offers significant advantages in terms of power consumption by operating in the sub-threshold region and by employing leakage reduction techniques such as dual-threshold voltage schemes, sleep transistors, body biasing, and clock gating [3]. These characteristics make it well suited for ultra-low voltage applications, especially in the biomedical domain, where speed is not as important as power efficiency. Due to the lower supply voltage and sub-threshold operation, the speed is limited to low-to medium-speed applications. Furthermore, the methods employed to lessen leakage and power consumption increase the complexity of the design [3]. In contrast, the 10-bit 50-MS/s asynchronous SAR ADC with 65 nm CMOS employs an innovative split-monotone DAC structure and asynchronous control logic that enables high-speed operation (50 MS/s) at low power consumption (2.79 mW) [4]. It achieves satisfactory results with an excellent signal-to-noise ratio (SNDR) and effective number of bits

DOI: 10.54254/2755-2721/89/20241075

(ENOB), making it ideal for high-performance applications. To reduce the comparator offset, the split DAC structure also stabilizes the common-mode voltage. However, the large layout area (350 μm×300 μm) and high complexity of this design may prove disadvantageous for some small applications [4].

3.2. Sigma-Delta (Σ-Δ) ADC

A sigma-delta ADC that consists of a fourth-order sigma-delta modulator and a fifth-order cascaded integrator comb (CIC) decimator filter is presented by Chen et al [5]. In order to lower quantization noise and improve loop stability, the modulator employs a multi-bit quantizer in a cascaded integrator feed-forward (CIFF) topology. The offset voltage of the comparator and the noise generated by kickback are reduced by neutralization and input offset storage (IOS), respectively [5]. The CIC decimator filter processes the output of the modulator, which includes high-frequency quantization noise, so as to remove the noise and prepare the output for use in other applications [5]. To minimize distortion due to charge injection and leakage currents, complementary T-switches are used in the sample-and-hold circuitry when designing a second-order sigma-delta ADC with complementary T-switches [6]. The architecture utilizes an off-chip digital extraction filter, a dynamic comparator, and a completely differential switching capacitor integrator, and employs a cascade-of-integrators feedback (CIFB) structure [6]. With the duty ratio principle, the ADC converts the voltage ratio of the front-end circuit, which carries temperature information, into a digital signal. The accuracy and integrity of the signal are improved by effectively reducing leakage current and charge injection effects, using a complementary structure of T-switches [6].

The study by Chen et al. Underscored the application of sigma-delta ADCs in automotive control systems, citing their high resolution, noise shaping capability, and energy efficiency [5]. The proposed ADC exhibits a high spurious-free dynamic range (SFDR) and signal-to-noise distorts ADC offers high spurious-free dynamic range (SFDR) and signal-to-noise-and-distortion ratio (SNDR) at a conversion rate of 1 MS/s, thereby meeting the rigorous standards required for automotive applications. Given the paramount importance of safety, controllability, and high reliability, these characteristics render them well-suited for incorporation into vehicle control systems that necessitate the conversion of accurate and reliable data [5]. Conversely, precision temperature sensors represent a significant application for sigma-delta ADCs with a complementary T-switch [6]. Due to the extensive operating temperature range and emphasis on avoiding distortion and leakage current, the ADC is well suited for low-frequency temperature signals [6]. The performance of the ADC in terms of ENOB and SNDR is improved by the complementary T-switch architecture, thereby facilitating its deployment in high-resolution temperature sensing applications within measurement, instrumentation, and control systems [6].

3.3. Flash ADC

According to Ignatius et al, the dynamic flash ADC design utilizes a fast thermometer encoder and a low-power open-loop comparator [7]. To ensure high-speed performance, this dynamic flash ADC is built using 180 nm technology and standard cells such as NAND, NOR, and INVERTER. While the dynamic thermometer encoder converts the analog input to binary output code without an intermediate stage, the dynamic Flash ADC architecture employs a pre-charge and evaluation phase to accomplish high-speed operation. The design is optimized for high speeds, where the dynamic encoder has the highest performance in its class to reduce latency and increase conversion speed [7]. Besides, the study by Megha et al. proposed to reduce power consumption and increase speed by reducing the number of comparators, where the N-bit ADC of the architecture uses only N comparators, whereas conventional implementations require 2n-1 comparators and an analog multiplexer to create the reference voltage. The applications that require rapid data conversion may benefit from the high-speed sample rates up to 2 GS/s, which are made possible by the reduction in comparators and the use of CMOS transmission gates [8]

The high-performance dynamic flash ADCs are implemented to achieve low power consumption by utilizing a dynamic temperature encoder and an open-loop comparator, which drastically reduces the number of transistors required, resulting in power and area savings [7]. The dynamic flash ADC,

DOI: 10.54254/2755-2721/89/20241075

designed using 180 nm technology, demonstrates lower static power dissipation due to the presence of footed NMOS transistors with lower static power consumption. This makes it suitable for real-time and mixed-signal systems where energy efficiency is critical [7]. In addition, Megha et al. placed greater emphasis on reducing the power consumption by reducing the number of comparators, and the proposed 4-bit ADC design requires only 4 comparators and multiplexers to generate the reference voltage, thus achieving significant power savings [8]. The approach employs 90 nm technology with a power consumption of 23 mW and an operating voltage of 1.2 V. This makes it particularly well-suited to small battery-driven devices, including tablets, cell phones, and portable medical devices, where portability and power economy are of paramount importance [8].

3.4. Other ADC Architectures

In addition to the three types mentioned above, there are two other types of ADCs, dual slope ADCs and pipeline ADCs, as described below.

The dual-slope ADC works by integrating the input voltage over a fixed period of time and then discharging it at a known rate. Initially, the input signal charges a capacitor for a specified duration, resulting in a voltage that is proportional to the input. Subsequently, the reference voltage discharges the capacitor, and the time taken to return to zero is measured. And the time is proportional to the input voltage. Known for their high accuracy and noise rejection, dual-slope ADCs are commonly used in digital multimeters. However, compared to other types of ADCs, dual-slope ADCs have relatively slow conversion speeds due to the need for integration.

The pipeline ADC, also known as a subranging ADC, uses a series of stages, each performing a portion of the conversion. Each stage resolves a few bits of the input signal, passes the residue (the difference between the input and its approximation) to the next stage for further processing. This process continues down the pipeline, with each stage working in parallel to increase throughput. Pipeline ADCs offer high-speed conversion and good resolution, making them ideal for applications in communication systems and video processing. However, their primary drawbacks are the complexity and latency introduced by the multiple stages.

4. Challenges and Strategies for ADC Design

4.1. Power Consumption

The design of ADCs with low power consumption is of paramount importance, especially for portable and battery-operated devices. Given that comparators are power-hungry components, an effective strategy is to reduce the number of comparators. For instance, a traditional flash ADC requires 2n-1 comparators for N-bit resolution, thereby consuming a considerable amount of power. The number of comparators can be significantly reduced by using a multiplexer to generate the reference voltage, as demonstrated in a low-power flash ADC design, where a 4-bit ADC uses only 4 comparators [8]. In addition, the design of dynamic flash ADCs with open-loop comparators and dynamic thermometer encoders can result in additional reductions in power consumption, achieved by minimizing the number of transistors and thus the overall power consumption [7].

4.2. Resolution and Accuracy

The enhancement of the resolution and accuracy of ADCs requires the identification and rectification of various sources of error, in addition to the deployment of sophisticated techniques. Therefore, minimizing power consumption while maintaining high resolution is one of the challenges. Techniques such as multi-bit quantization and the integration of advanced filtering mechanisms like CIC filters can help achieve this balance. For example, Sigma-Delta ADCs use oversampling and noise shaping to enhance resolution, rendering them well-suited for high-precision applications [5]. Another approach is the use of IOS and comparator offset neutralization to reduce errors and improve accuracy in ADC designs [5].

DOI: 10.54254/2755-2721/89/20241075

4.3. Trade-offs between Speed and Complexity

Achieving high-speed conversion in ADCs while maintaining accuracy and low power consumption is a significant challenge. High-speed ADCs, such as pipeline ADCs, divide the conversion process into several stages, allowing for parallel processing and faster conversion times. However, this introduces complexity and latency. Dynamic flash ADCs employ fast thermometer encoders and dynamic logic to achieve high-speed performance, with designs optimized for low power and high-speed operation. For instance, they can achieve sampling rates up to 2 GS/s with reduced delay and power dissipation [8]. The design of such devices necessitates a careful consideration of the trade-offs between speed, resolution, and power efficiency, as well as the development of innovative circuit architectures.

5. Conclusion

This paper delves into the fundamentals, types, performance metrics, and recent advances in ADC technology, and evaluates their respective advantages and limitations by examining their operational mechanisms, such as SAR, Sigma-Delta, and flash ADCs. In addition, the results demonstrate that power efficiency is a crucial consideration, particularly for portable and battery-powered devices; techniques such as reducing the number of comparators and using dynamic logic can significantly reduce power consumption, making ADCs suitable for low-power applications; and improving resolution and accuracy requires addressing sources of error through advanced techniques such as multi-bit quantization and integrated filtering mechanisms.

In conclusion, the uninterrupted advancement of ADC technology is of paramount importance for meeting the ever-evolving demands of digital systems. To address the challenges related to power consumption, resolution, and speed, it is necessary to adopt innovative approaches in both material science and circuit design. Future research should concentrate on integrating emerging technologies such as AI in order to dynamically optimize ADC performance. The proliferation of IoT devices necessitates the development of ADCs that are not only highly efficient but also capable of operating in a multitude of environments. The future ADCs will challenge the boundaries of current technology, potentially attaining unparalleled levels of efficiency and performance to guarantee their continued relevance and applicability in an increasingly digital world.

References

[1] Zamaruiev, V.V. (2017) The Use of Kotelnikov-Nyquist-Shannon Sampling Theorem for Designing of Digital Control System for a Power Converter. 2017 IEEE First Ukraine Conference on Electrical and Computer Engineering (UKRCON), pp. 522-527.

[2] Ren, J., Xiong, J. and Liu, J. (2018) High-Speed ADC Quantization with Overlapping Metastability Zones. 2018 IEEE 61st International Midwest Symposium on Circuits and Systems (MWSCAS), pp. 234-237.

[3] Majidi, R. (2023) Low Power Design of Successive Approximation Registers. 2013 21st Iranian Conference on Electrical Engineering (ICEE), pp. 1-6.

[4] Zhao, J., Huang, Z. and Hou, X. (2022) A 10-bit 50-MS/s Asynchronous SAR ADC in 65nm CMOS. 2022 IEEE 14th International Conference on Advanced Infocomm Technology (ICAIT), pp. 225-229.

[5] Chen, Y., Wang, Z., Zhuang, Y. and Tang, H. (2021) Analysis and Design of Sigma-Delta ADCs for Automotive Control Systems. 2021 IEEE 3rd International Conference on Circuits and Systems (ICCS), pp. 235-241.

[6] Guo, Y,. Jin, J., Liu, H. and Huang, J. (2021) A Sigma-Delta ADC with Complementary T-Switch," 2021 6th International Conference on Integrated Circuits and Microsystems (ICICM), pp. 380-383.

[7] Ignatius, T.M., Antony, J.K. and Mary, S.R. (2014) Implementation of high performance dynamic flash ADC. 2014 Annual International Conference on Emerging Research Areas: Magnetics, Machines and Drives (AICERA/iCMMD), Kottayam, India, 2014, pp. 1-5.

DOI: 10.54254/2755-2721/89/20241075

[8] Megha, R. and Pradeepkumar, K.A. (2014) Implementation of Low Power Flash ADC by Reducing Comparators. 2014 International Conference on Communication and Signal Processing, pp. 443-447.