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Design and Analysis of Miller Compensated Two-Stage Operational Amplifier

Yuheng Zou

School of Information Science and Technology, North China University of Technology Beijing, 100144, China

21152040102@mail.ncut.edu.cn

Abstract. With the development of integrated circuit technology, the size of electronic equipment continues to reduce, and speed continues to increase. Operational amplifiers are the key circuit in analog ICs, and the required performance of operational amplifiers is also increasingly high, research and design of high-performance operational amplifiers has become one of the key topics of today's research. A CMOS two-stage operational amplifier with high unity-gain bandwidth is analysed and designed with an appropriate Miller-compensation technique in this research to improve the frequency characteristics and stability. The design is based on 180nm CMOS process. Its performance is simulated and analysed in Cadence software environment. The performance parameters are shown by simulation results that the amplifier has a gain of 61.81dB, a GB (unity-gain bandwidth) of 907.42MHz and a phase margin of 75.02°. The experimental results show that it achieves high unity-gain bandwidth while ensuring gain and stability. Through this study, the principles of two-stage operational amplifiers and their compensation as well as the design and simulation are shown in detail in both theoretical and experimental sections.

Keywords: Operational amplifier, two-stage, stability, Miller-compensation, CMOS-design.

1. Introduction

Operational amplifiers are fundamental components in various applications, including analog, digital, and mixed-signal circuits. They serve as crucial building blocks for ADCs (analog-to-digital converters), DACs (digital-to-analog converters), signal processing systems and automatic control systems etc. Additionally, they are essential for higher-order active filters, signal amplification, and ultra-high-speed signal conversion [1]. The overall performance of integrated circuits incorporating operational amplifiers heavily relies on the capabilities of these amplifiers.

An ideal operational amplifier should provide infinite bandwidth, infinite input impedance, infinite open-loop gain, infinite output voltage swing, infinite swing rate, infinite common-mode rejection ratio (CMRR), infinite power supply rejection ratio (PSRR), zero output impedance, and other characteristics.

In reality, however, the ideal operational amplifier does not exist due to manufacturing process deviations, parasitic effects, noise, and non-ideal characteristics of semiconductor devices. These realistic problems affect the performance of the amplifier, making it difficult to combine the various performances of operational amplifiers.

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Therefore, when designing operational amplifiers, these non-ideal characteristics need to be taken into account. According to the actual needs of the applied scenarios, the appropriate performance indexes should be selected. The indexes should be designed with a balance and appropriate compensation and optimization.

The single-stage operational amplifier's input transistor produces a small signal current that flows directly through the output impedance, only one voltage-to-current conversion is performed. As a result, the gain of a single-stage amplifier is constrained by the product of the transconductance of the input transistors and the output impedance. While implementing a cascode structure can enhance the gain, it also limits the output swing [2]. Design of multistage operational amplifiers is more complicated. It introduces multiple poles and zeros, making compensation techniques difficult to design for high speeds and large bandwidths. Its other disadvantages include higher power consumption, larger circuit size and interference effects.

Overall, the two-stage operational amplifier structure offers a compromise. It is more widely used than single and multistage structures, due to its relatively simple structure and better performance parameters.

In some past researches, Y. Yang et al. introduced an efficient and optimized design approach for two-stage Miller-compensated operational amplifiers. They employed a neural network model to capture the relationship between op-amp parameters and performance metrics, significantly enhancing simulation efficiency [3]. C.Krithika et al. designed and simulated a high-performance CMOS two-stage amplifier using an improved Miller-compensated methodology, which was carried out in the 90nm simulation design environment of Cadence tool software. Achieved 194MHz unity-gain bandwidth, 10.8V/μS slew rate, 76dB gain and 106.3μW low power consumption and 70° phase margin [4]. Y. R. Gandweed et al. used a power gating technique to optimize the problem of high-power consumption of the two-stage operational amplifier. Two additional head transistors are connected in parallel in the circuit. The power supply to the amplifier can be turned off when the amplifier is not in use, such as during idle periods or when the input signal voltage falls below a threshold value [5]. X. Jin and J. He designed a two-stage differential op-amp using a 180nm CMOS process. It achieves a gain of 85.5dB, CMRR and PSRR are both approximately 90dB, and a Miller compensation is used to achieve a phase margin of 80° [6]. M. A. Chaudhry designed an operational amplifier operating at 0.8V single supply with 0.12μm process technology, which uses a folded cascode design to optimize the output signal voltage swing at low VDD [7].

This paper describes in detail the principle, structure, and design method of CMOS two-stage operational amplifier. It particularly focuses on the principle of stability optimization using Miller compensation and nulling resistor. The study presents the design of a Miller-compensated two-stage operational amplifier that has a high unity-gain bandwidth and demonstration of performance parameters obtained through simulation and analysis. Finally, the study concludes with a summary of the designed CMOS two-stage operational amplifier is summarized.

2. Theoretical Analysis

This section contains a theoretical analysis of two-stage operational amplifiers. It includes the function of each component, and the theory needed in the design.

2.1. Two-stage operational amplifiers

A Miller compensated two-stage op-amp is a widely used circuit structure designed to achieve high gain and better phase margins in the design of amplifiers [8]. A two-stage op-amp consists of two amplifiers cascaded together. The first stage of the circuit is a differential amplifier that delivers high gain, while the second stage is a common-source amplifier responsible for providing a wide output swing.

Two-stage op-amp achieves good balance between high gain, large output swing and bandwidth. Figure 1 shows the circuit structure of a typical two-stage operational amplifier. The transistors $M_1 \sim M_5$ consist a differential amplifier as first stage, M_1 M_2 provides the differential input to the op-amp, and this differential structure provides better suppression of common-mode disturbances.M_3 M_4 is a current-

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mirror active load, and M_5 is a tail-current source providing a stable current bias to the first stage. The second stage is a common source amplifier consisting of transistors M_6 M_7. The current source and M_0form a bias circuit and the current flows through the diode connected M_8 to generate a bias voltage at the gate.

Signals from the first stage are fed into the second stage, which is amplified by M6. Miller capacitor C_C and nulling resistor R_C are connected with the output node of the first stage and second stage as a compensation circuit for adjusting the zero pole to improve stability.C_L is used as the output capacitance load of the op-amp.

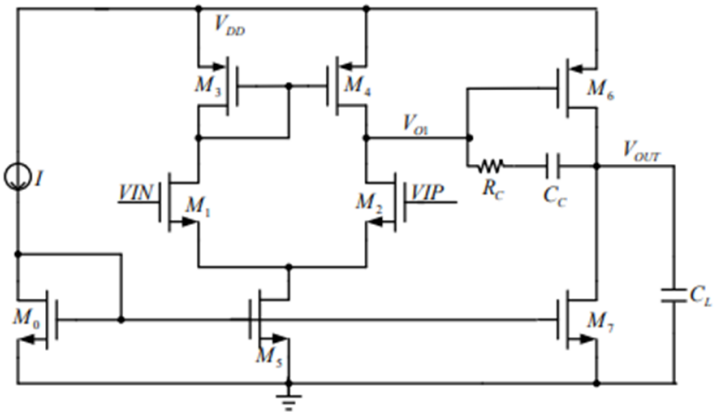

Figure 1. Two-stage operational amplifier schematic.

2.2. Design methodology

The design process for an operational amplifier involves translating performance requirements into a specific topology structure, transistor size and compensation method. The structure of the operational amplifier is firstly chosen based on the key performance criteria. Then the schematic of circuit with all transistor connections are drawn. Next, the aspect ratio of each transistor in the operational amplifier is calculated manually after clarifying the relevant process parameters. Finally, simulation is carried out by using the software, and adjustments are made according to the results. A two-stage amplifier structure has been selected for this study. A series of performance specifications are given below in relation to the parameters.

The formula for gain is shown in (1), the first stage gain A_{v_1} multiplied by the second stage gainA_{v_2} is the total gain A_v, which is the gain of the two stages as in formula. Equation (2) is the formula for the unity-gain bandwidth, reflecting the frequency when the amplifier gain is reduced to 0dB. Equation (3) is the relationship that needs to be satisfied in order to meet a phase margin greater than 60°.

$$A_v = A_{v_1} A_{v_2} = \frac{g_{m1} g_{m6}}{(g_{ds2}+g_{ds4})(g_{ds6}+g_{ds7})} \tag{1}$$

$$GB = \frac{g_{m1}}{C_C} \tag{2}$$

$$C_c > 0.22 C_L \tag{3}$$

The transfer function of the two-stage op-amp that is uncompensated has two poles and the frequency positions of the poles are located before the unity-gain bandwidth is reached. In addition, the presence of multiple poles in a circuit can led to instability. So, uncompensated two-stage op-amps typically have a phase margin of less than 40°. In order to improve stability, the phase margin of the op-amp should be at least greater than 45° and preferably greater than 60°. Therefore, it is crucial to introduce frequency compensation circuits into operational amplifiers to ensure their stable operation at all operating conditions. In this design, the Miller effect is used for pole separation.

Figure 2 shows the distribution of zero poles before and after compensation, figure 3 shows the baud plot before and after compensation [9], equations (4) ~ (6) are the zero poles after Miller compensation,

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and the equations reflect the relationship between C_C and the position of zero poles. Combining the amplitude-frequency curve and phase frequency curve in the baud plot, it can be seen that after Miller compensation, the original two poles p_1' and p_2' are separated to both sides and moved to the positions of p_1 and p_2, while the zero z_1 is introduced.

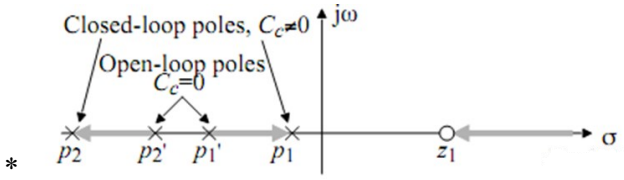

Figure 2. Comparison of zero poles before and after compensation [9].

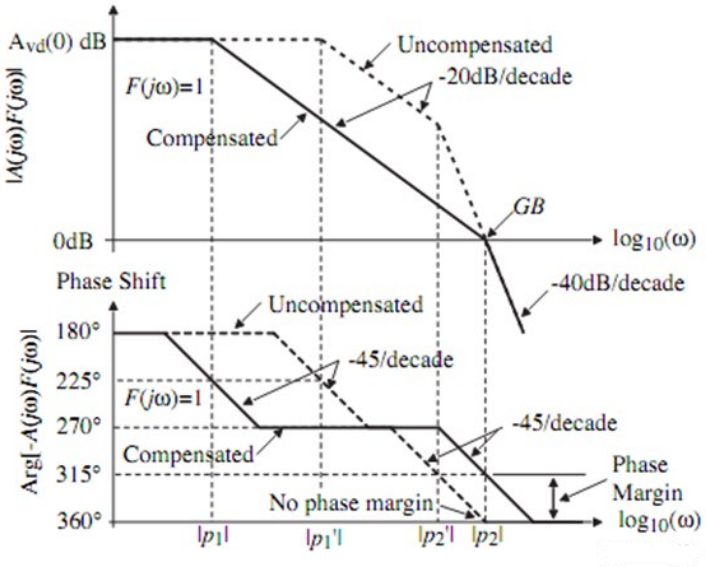

Figure 3. Baud plot before and after compensation [9].

$$z_1 = \frac{g_{mII}}{C_C} = \frac{g_{m6}}{C_C} \tag{4}$$

$$p_1 \cong \frac{-1}{g_{mII}R_IR_{II}C_C} \cong \frac{-(g_{ds2}+g_{ds4})(g_{ds6}+g_{ds7})}{g_{m6}C_C} \tag{5}$$

$$p_2 \cong \frac{-g_{mII}C_C}{C_IC_{II}+C_CC_I+C_CC_{II}} \cong \frac{-g_{m6}}{C_L} \tag{6}$$

While applying Miller compensation, due to the presence of Miller capacitance, there are two feedforward paths at the output node. At a certain complex frequency, if the signals passing through these two paths are equal in magnitude but opposite in phase, they cancel each other out. This cancellation introduces a RHP (right half-plane) zero z_1. The zero z_1 has no direct effect on system stability, but the system may become unstable due to the position of the two poles as the phase lag due to this pole reduces the phase margin. To eliminate the RHP zero, the use of a nulling resistor needs to be considered. A nulling resistor R_z, is connected in series with the branch on which the Miller compensation capacitor is located. The nulling resistor introduces a weaker third pole in the system, but it is able to push the RHP zero away from the main pole of the system. The positions of pole $p_1$and pole p_1 remain almost constant [10]. The expressions for the zero z_1 and pole p_3 are shown by equations (7) and (8).

$$z_1 = \frac{1}{C_C(\frac{1}{g_{mII}}-R_Z)} \tag{7}$$

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$$p_3 = -g_{mII}(\frac{1}{C_I} + \frac{1}{C_C} + \frac{1}{C_L}) \tag{8}$$

It is easy to see that the position of the zero z_1 can be moved by adjusting the value of R_z. Typically, to eliminate the effect of RHP, adjusting R_z moves the RHP zero farther away than GB, or to a position p_2 with respect to the load capacitance with the poles cancelled out.

3. Simulation

Table 1 shows the design requirements of the op-amp in this design, where the required supply voltage is 3.3V, the unity-gain bandwidth should be more than 800MHz, the gain is more than 60dB, and the phase margin is more than 60°. The schematic diagram of the two-stage operational amplifier designed and drawn with Cadence software using the 180 nm CMOS process is shown in figure 4.

Table 1. Operational amplifier design requirements.

Performance parameters	Performance requirements
ICMR	3V
Power consumption	⩽20mW
Gain	⩾60dB
GB	⩾800MHz
Phase margin	⩾60°
CMRR	⩾60dB
PSRR	⩾70dB

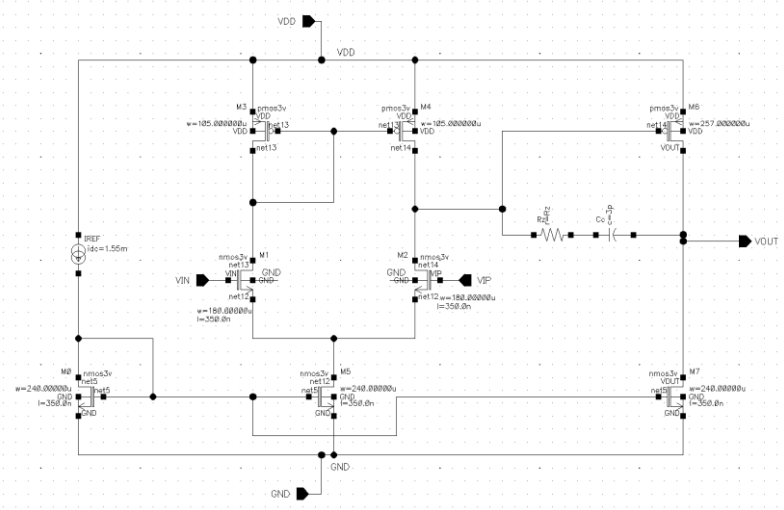

Figure 4. Schematic of designed two-stage amplifier.

3.1. DC analysis

The DC analysis includes ICMR and output swing. To test the ICMR, the operational amplifier is configured in a unity-gain feedback loop as figure 5. The voltage input in the positive input terminal is swept from 0V to VDD while observing the output voltage response. The linear range can be observed from the output voltage versus input voltage curve. In the linear operating region of the amplifier, the slope of the DC sweep curve is 45°, indicating that the output can effectively follow the input. If the input exceeds the linear range, the curve bends. The final simulation results are shown in figure 6, where the boundary points of the linear region are identified. The simulation concludes that the ICMR is 3.102V.

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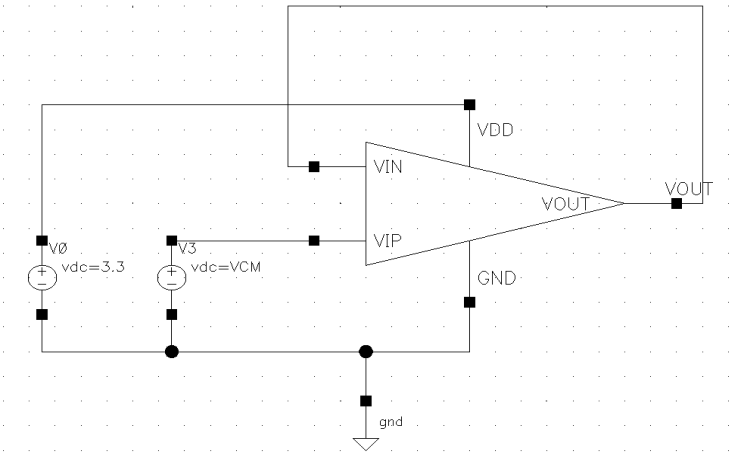

Figure 5. ICMR test circuit.

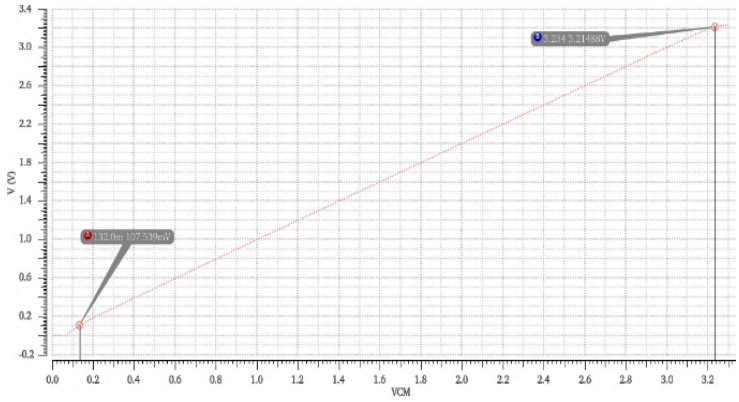

Figure 6. ICMR test result.

To test the swing, the designed amplifier is connected to the structure shown in figure 7, which voltage gain is -10. The positive input of the op-amp is connected to VDD/2 to provide the op-amp with a common-mode input in the center of power supply rails, and a DC sweep from 0 to VDD is performed on the negative input, and the portion of the output voltage that varies linearly is the swing under this power condition. The result of the voltage swing is obtained as shown in figure 8, which gives the swing range: 317.075mV-3.00137V.

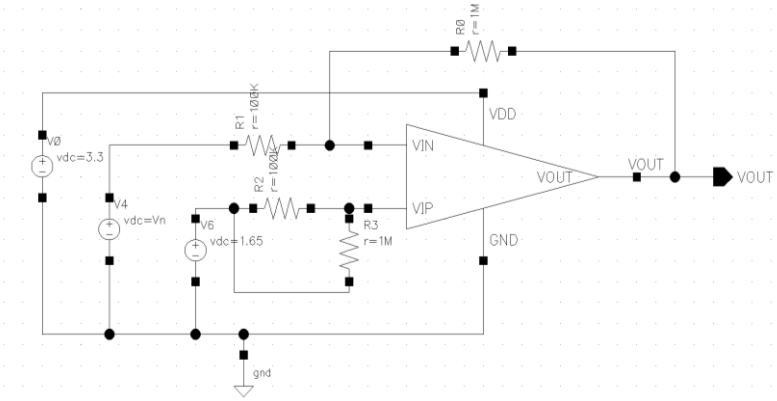

Figure 7. Swing test circuit.

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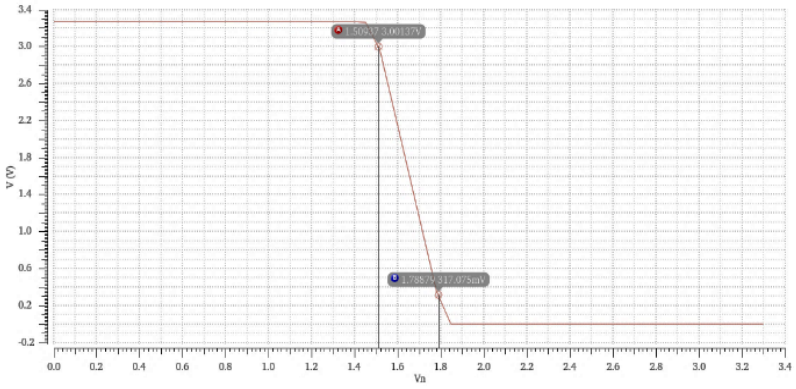

Figure 8. Swing test result.

3.2. AC Analysis

AC analysis mainly tests frequency-related parameters, including gain, GB, phase margin, CMRR and PSRR.

3.2.1. Open loop frequency response

Due to the op-amp has a very high open-loop gain, the circuit is very sensitive to adaptation, making it difficult to measure the gain using an open-loop method directly. Therefore, common-mode feedback is applied to stabilize the output voltage of common-mode stage. The test circuit, as shown in figure 9, is designed as a practical circuit for measuring the open-loop AC parameters.

In the test circuit, the resistor (R0) and capacitor (C2) form a low-pass feedback network with very large values, ensuring that the cutoff frequency is much lower than the operational amplifier's dominant pole frequency. This configuration makes the DC levels of the positive and negative input terminals equal, with the negative input terminal AC-grounded. CL represents the expected load for the operational amplifier. A sinusoidal input signal with a magnitude of 1V, and an AC sweep is performed over a frequency range of 0.1Hz to 10GHz. The test results, as shown in figure 10, indicate that the operational amplifier has a GB of 907.42MHz, a phase margin of 75.02°, and a gain of 61.80dB.

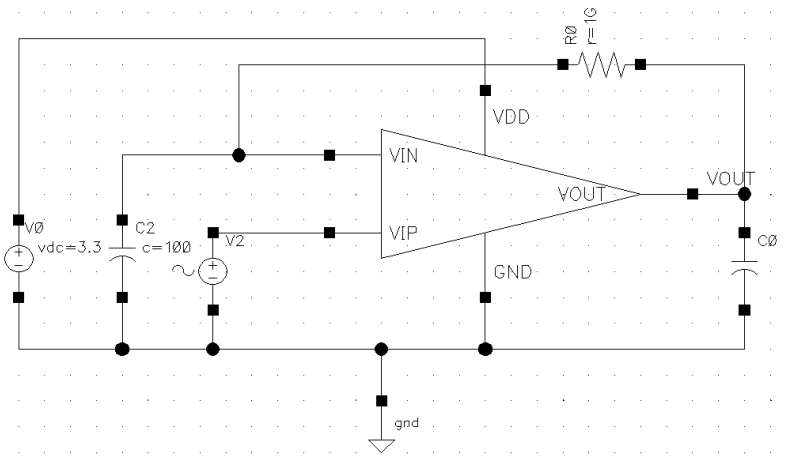

Figure 9. Frequency response test circuit.

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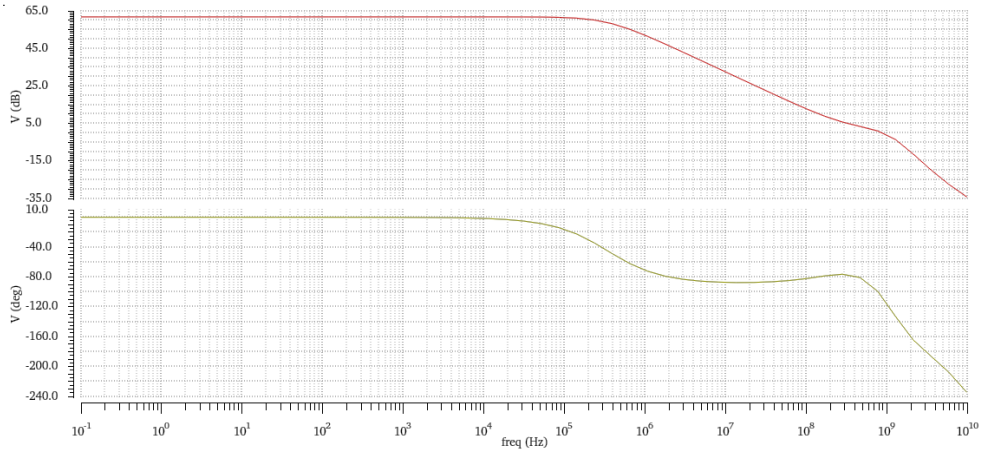

Figure 10. Amplitude-frequency and phase-frequency curves.

3.2.2. CMRR

Figure 11 shows the CMRR test circuit, the op-amp is connected as a unit negative feedback structure, a unit AC small signal source vcm is added between the output and the negative input, and the same signal is added to the positive input; the VCM provides the circuit with a DC operating point, and the CMRR can be obtained by performing an AC frequency sweep of the structure as shown in figure 11, and the CMRR of this op-amp is about As shown in figure 12, the CMRR of this designed op-amp is about 60.44dB.

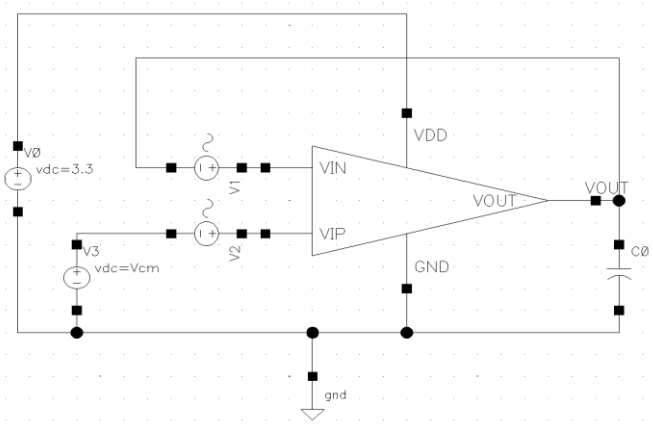

Figure 11. CMRR test circuit.

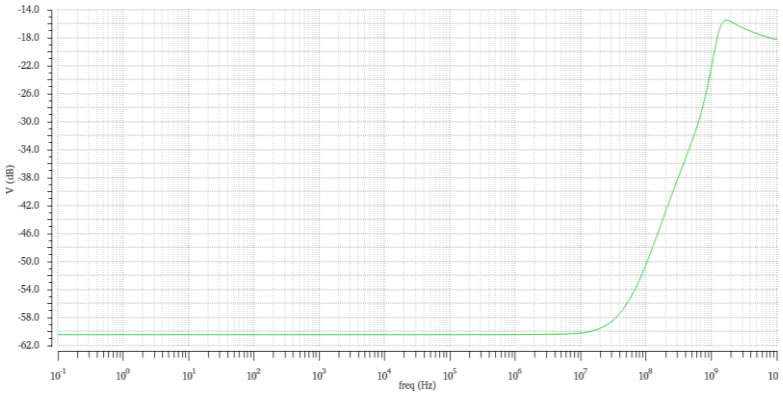

Figure 12. CMRR test result.

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3.2.3. PSRR

Figure 13 shows the PSRR test circuit, which is similar to the simulation of CMRR, connecting the op-amp into the form of a unit of negative feedback, and adding a unit of AC component to the supply voltage, performing AC frequency scanning, and observing the frequency response of the output to obtain PSRR, and the test results are shown in figure 14, with a PSRR of about 70.01dB.

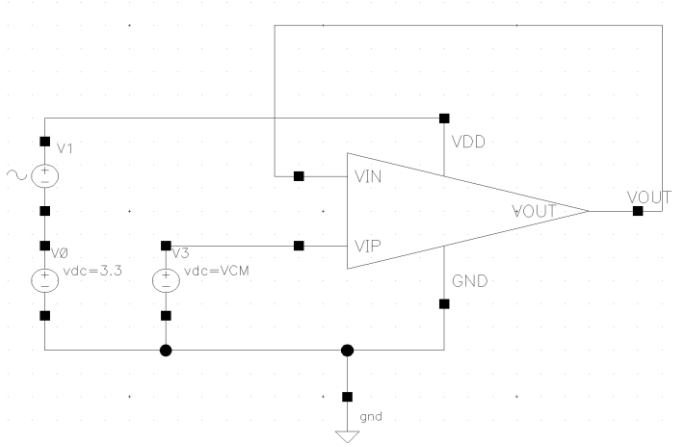

Figure 13. PSRR test circuit

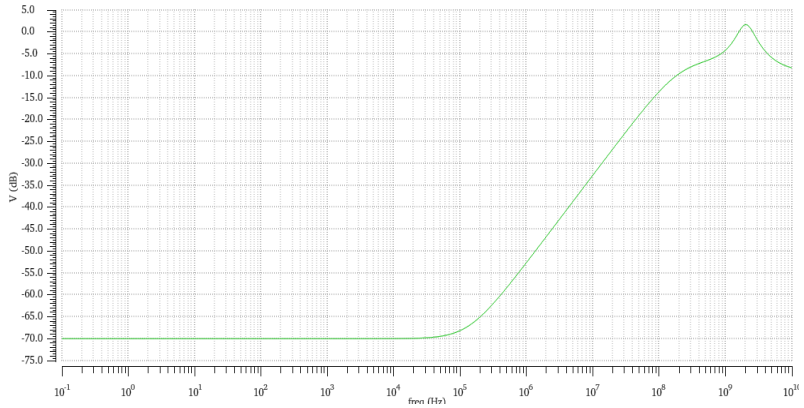

Figure 14. PSRR test result

3.3. Results

Table 2. Comparison of simulation results and performance requirements.

Performance Parameters	Performance Requirements	Simulation Results
ICMR	3V	3.102V
Power Consumption	⩽20mW	15.53mW
Gain	⩾60dB	61.80dB
GB	⩾800MHz	907.42MHz
Phase Margin	⩾60°	75.02°
CMRR	⩾60dB	60.44dB
PSRR	⩾70dB	70.01dB

Table 2 shows that the amplifier of this design achieves better-than-designed performance in terms of common-mode input range, swing, gain, unity-gain bandwidth, phase margin, CMRR, and PSRR.

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4. Conclusion

In this paper, based on the application of operational amplifiers, the research background, principle, design, and simulation and verification methods of two-stage operational amplifiers are described in detail. And a two-stage op-amp with 907.42MHz high unity-gain bandwidth is designed and simulated using Cadence Virtuoso tool in 180nm CMOS process to improve the unity-gain bandwidth by varying the width of the transistors, and increasing the current. Bandwidth and stability related issues are improved by nulling resistors and Miller capacitors. Successfully realized a two-stage op-amp that is better than the design requirements.

In future research, new circuit topologies, compensation means and more efficient design methods can be explored to further optimize and improve the performance metrics such as gain, bandwidth, power consumption, stability, and the balance between them.

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