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A Method for Reducing Offset in CMOS Operational Amplifiers

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Abstract: In the development of integrated circuits, operational amplifiers are indispensable basic units CMOS operational amplifiers are the core components in analog integrated circuits, which are widely used in signal acquisition, data processing, communications and other fields. components in analog integrated circuits, which are widely used in signal acquisition, data processing, communications and other fields, and their performance has a direct impact on the accuracy and stability of the entire system. With the continuous development of electronic technology, CMOS operational amplifiers play a vital role. operational amplifiers play a vital role in many fields. However, the misalignment problem has been one of the key factors affecting the performance of However, the misalignment problem has been one of the key factors affecting the performance of CMOS operational amplifiers. This paper introduces the basic principles of CMOS operational amplifiers, thoroughly studies the phenomenon of CMOS operational amplifiers' misalignment. This paper introduces the basic principles of CMOS operational amplifiers, thoroughly studies the phenomenon of CMOS operational amplifiers' misalignment, the definition and sources of the misalignment voltage and its effects, and analyzes the main reasons for its generation, including device mismatch, process deviation, and so on. In this paper, we summarize several methods to reduce distortion from dynamic distortion elimination technology and design and process optimization, which can effectively reduce the distortion voltage of CMOS op amps. The main dynamic misalignment elimination techniques are chopping and auto-zeroing, as well as a special form of auto-zeroing, i.e., correlation dual- sampling technique. Design and process optimization includes two methods of device selection and matching optimization and circuit topology design.

Keywords: operational amplifier, CMOS, offset voltage

1. Introduction

Operational amplifiers are the most important and basic devices in integrated circuits, which are widely used in today's industrial production, and are mainly applied in many fields such as sensor signal processing, communication systems, medical instruments, and automatic control. In these applications, the precision and stability of operational amplifiers are directly related to the performance of the whole system. With the development of electronic information systems towards low power consumption and low supply voltage, the performance requirements of operational amplifiers are getting higher and higher. As an important factor affecting the precision of CMOS

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operational amplifiers, distortion can cause the output signal to deviate from the ideal value, reducing the reliability and accuracy of the system. As one of the key performance indexes of CMOS operational amplifiers, the misalignment has a significant impact on their system amplification accuracy. Operational amplifier misalignment is mainly divided into two categories: random misalignment and systematic misalignment. For random misalignment, the optimization of circuit matching can be taken to reduce the misalignment, while for systematic misalignment, the gain of the op-amp should be ensured to reduce the impact of misalignment [1]. Therefore, it is of great practical significance to study the distortion reduction techniques of CMOS operational amplifiers. In this paper, we will deeply analyze the distortion mechanism of CMOS operational amplifiers based on CMOS process and study various methods to reduce the distortion.

The first chapter of this paper is the introduction part, which introduces the research background and research significance of the thesis, and lays the foundation for the whole paper; the second chapter is the basic principle and the mechanism of CMOS op-amps, which is divided into three subsections, which introduces the basic principle of CMOS op-amps, the definition and the source of distortion voltage, and the effect of the distortion voltage, respectively; the third chapter is the method of reducing the distortion of CMOS op-amps, which is divided into two sections, 3.1 investigates two dynamic distortion elimination techniques, i.e., chopping technique and auto-zeroing technique. divided into two sections, 3.1 investigates two dynamic distortion elimination techniques, i.e., chopping technique and auto-zeroing technique, and 3.2 mainly talks about the methods to reduce the distortion by optimizing the design and process of op-amps, i.e., two methods, i.e., the optimization of device selection and matching and the circuit topology design. Through theoretical analysis and simulation experiments, this paper proposes a series of effective methods to reduce the distortion, which provides a reference for the design of operational amplifiers.

2. Fundamentals of CMOS Operational Amplifiers and Dissonance Mechanisms

2.1. Fundamentals of CMOS Operational Amplifiers

CMOS operational amplifier is a kind of analog circuit device fabricated by CMOS process, which realizes signal amplification and processing through differential input, differential output and voltage gain, etc. Its core part usually consists of differential pair tube, gain stage and output stage [2]. Differential pair tubes are responsible for receiving input signals and converting them into current signals; the gain stage realizes signal amplification by means of current mirrors or common source and common gate structures; and the output stage converts the amplified current signals into voltage signals for output [3].

2.2. Definition and Sources of Offset Voltage

An out-of-phase voltage is a non-zero voltage present at the output of an op-amp when the two input voltages are equal. The distortion voltage is an important parameter of an operational amplifier, which represents the voltage at which the output signal deviates from the ideal zero value under ideal conditions when the input signal is zero. The generation of the distortion voltage mainly comes from the following sources:

1. device mismatch: in CMOS process, due to process deviations and temperature variations, the parameters of the device (e.g., threshold voltage, mobility, etc.) are subject to certain variations, which lead to mismatch of the differential pair of tubes, thus generating an out-of-phase voltage [4].

2. Instability of the bias circuit: The bias circuit is used to provide a stable bias current and voltage for the operational amplifier, but it may itself be affected by temperature, power supply fluctuations, and other factors, resulting in bias point offset, which in turn generates an out-of-regulation voltage.

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3. Circuit Layout and Wiring: The layout and wiring in a circuit can also have an effect on the distortion voltage. For example, asymmetry in the layout of the differential pair of tubes, parasitic capacitance between the signal line and ground, etc., may introduce additional distortion voltages.

2.3. Effect of Offset Voltage

The presence of a distortion voltage can have a significant impact on the performance of an op amp. Firstly, the distortion voltage will directly cause deviation of the op amp signal and reduce the accuracy of the system; secondly, in closed-loop applications, the distortion voltage may cause the system to fail to work properly or to produce a large error. In addition, the detuned voltage may also cause nonlinear distortion of the system, which affects the overall performance of the system. Therefore, it is of great significance to study how to reduce the offset voltage of CMOS operational amplifiers.

3. Methods to Reduce the Misalignment of CMOS Operational Amplifiers

3.1. Dynamic Misalignment Elimination Technique

The advantage of CMOS process is lower cost and easy to integrate, which occupies an important position in the design of integrated circuits, but once used to design high-precision circuits, its out-of-phase voltage will have a significant impact on the whole system. It has been found that dynamic misalignment elimination technology is an important solution to reduce the misalignment, and there are two main types of technology, such as chopper technology and automatic zeroing technology.

3.1.1. Chopper technology

Chopping technique (CHS) is an important technique for eliminating the distortion voltage, the basic principle of which is to modulate the low-frequency noise and DC distortion voltage at high frequency by introducing a high-frequency modulating signal at the input of the operational amplifier, subsequently amplifying and demodulating the transmitted signal back to the baseband, and finally filtering out the high-frequency noise and the distortion voltage with a low-pass filter to achieve the reduction of the distortion voltage [5]. Chopping technique is an effective method to reduce the distortion voltage, which not only reduces the distortion voltage but also effectively suppresses the low frequency noise of CMOS operational amplifiers compared to other techniques [6].

Suppose the input signal is V_{in}, and the distortion voltage is V_{os} The signal after chopper modulation can be expressed as $V_{chop} = V_{in} + V_{os}$. After some high frequency chopper functionf(t) The result after modulation.

After demodulation, the output signalV_{out} can be approximated as $\mathrm{V_{out}} = \mathrm{g(V_{in} + V_{os})}$, where the function g represents the demodulation and subsequent processing. By rationally designing the chopping frequency, modulation and demodulation methods, etc., it is possible to make theV_{os} the effect of the chopping frequency in the V_{out} the influence of the.

3.1.2. Auto-zeroing techniques and associated dual sampling techniques

Auto-zeroing technique (AZ) is a method of calibrating the op-amp's offset voltage by periodically calibrating the op-amp. The core principle is to first sample the op-amp's noise and offset voltage, monitor and adjust the op-amp's offset voltage in real time by using specific calibration circuits and algorithms, and then subtract the offset voltage portion instantly from the op-amp's input or output so that it is kept at a low level [7]. Auto-zeroing techniques can significantly improve the accuracy and stability of op-amps, but may increase circuit complexity and power consumption.

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Suppose the ideal output of the circuit is V_{ideal} , the actual output is V_{actual} and the out-of-phase amount is V_{offset} and the input signal is V_{in}. In the sampling dissonance stage: when the input is shorted, the $V_{actual} = V_{offset}$, sample and store this value; in the stage of accessing the input signal, the circuit outputs $V_{actual} = V_{in} + V_{offset}$; after automatic zero compensation, the $V_{corrected} = V_{actual} - V_{offset} = V_{in} + V_{offset} - V_{offset} = V_{in}$, i.e., the removal of the distortion from the output is realized, making the output closer to the ideal input signal response.

The correlated dual sampling technique is a special form of the auto-zeroing technique and, as the name suggests, the principle differs in that the noise and the out-of-phase voltage need to be sampled twice in one clock cycle [8]. The correlated double sampling technique is performed twice in both the acquisition and holdover sessions, but the distortion voltages introduced by this technique are very similar to the auto-zeroing technique, and therefore the two techniques are discussed in the same category.

3.2. Design and process optimization

By optimizing the design parameters and fabrication process of the op-amp, it is possible to reduce the out-of-phase voltage to some extent. Selection of suitable devices in CMOS process and circuit topology design in op-amps are also important methods to reduce the out-of-phase voltage.

3.2.1. Device Selection and Fit Optimization

In CMOS processes, choosing the right device type and size is the basis for reducing the mismatch voltage. For example, low-noise, high-precision MOSFETs are used as differential pair tubes; mismatch is reduced by optimizing device geometry and layout. In addition, digital trimming techniques can be used to further reduce the misalignment voltage. Digital trimming techniques utilize digital latches and time clocks to control the current mirror array to compensate for the magnitude of the current and fine-tune the distortion voltage in the excessive region to achieve low distortion. The digital trimming technique not only improves the precision of operational amplifiers compared to other methods of reducing the distortion, but also meets the needs of low-cost and high-volume industrial production [9].

3.2.2. Circuit Topology Design

Circuit topology design is the key to reduce the out-of-phase voltage. In the design of CMOS operational amplifiers, commonly used circuit structures include folded common source and common gate structures, sleeve structures, and so on. These structures need to consider the optimization of power consumption, noise and other performance indicators while achieving high voltage gain. For example, the folded common-source common-gate structure increases gain and stability by introducing additional common-source common-gate stages, but also increases power consumption and noise [10]. Therefore, the optimal circuit topology needs to be selected in the design by comprehensively considering various performance metrics.

4. Conclusion

4.1. Summarizing the results

Operational amplifiers are crucial in integrated circuits and are widely used in several fields. CMOS operational amplifiers, as the core components of analog integrated circuits, have performance that affects the accuracy and stability of the whole system. The misalignment problem is one of the key factors affecting the performance of CMOS operational amplifiers.

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This paper introduces the basic principles of CMOS operational amplifiers, including its composition of differential pair of tubes, gain stage and output stage, which realizes signal processing through differential input, differential output and voltage gain. At the same time, an in-depth study of the out-of-phase voltage, which is defined as the non-zero voltage at the output of the op-amp when the voltages at the two inputs of the op-amp are equal, the sources of which include device mismatch, unstable bias circuits, as well as circuit layout and wiring, etc., out-of-phase voltages can reduce the accuracy of the system, affect the closed-loop applications and lead to nonlinear distortion.

In order to address the problem of misalignment, this paper summarizes a variety of methods to reduce misalignment. In terms of the dynamic dissonance elimination techniques, the chopper technique and the automatic zeroing technique and its special form of related double sampling technique are introduced. Chopper technology through the introduction of high-frequency modulation signal at the input, the modulation of the distortion voltage to high-frequency and then demodulated and filtered to reduce the distortion, but also to suppress low-frequency noise; automatic zeroing technology through the regular calibration of the op-amp distortion voltage, the instantaneous subtraction of the part of the distortion voltage at the input or the output side of the accuracy and stability, and the associated double sampling technology in a clock cycle on the noise and the distortion voltage sampling twice. In terms of design and process optimization, it includes device selection and matching optimization as well as circuit topology design. Device selection can be used as a low-noise, high-precision MOSFET differential pair of tubes and optimize the geometry and layout, but also the use of digital trimming technology; circuit topology design needs to take into account the performance indicators, such as folded common source and common gate structure can increase the gain and stability, but it will increase power consumption and noise.

Through the above research, this paper provides a series of effective methods for the design of CMOS operational amplifiers to reduce the distortion, which is an important reference value for improving the performance of operational amplifiers.

4.2. Future Prospects

4.2.1. Optimization of Existing Dimming Techniques

Chopping technique: further study the optimal combination of chopping frequency, modulation and demodulation methods to achieve more efficient distortion voltage reduction and lower low-frequency noise suppression. Explore how to adaptively adjust the chopping parameters according to different application scenarios and circuit requirements to improve the versatility and flexibility of chopping technology.

Auto-zeroing technology and related dual-sampling technology: study how to further improve the accuracy and stability of auto-zeroing technology without significantly increasing circuit complexity and power consumption. For the related dual sampling technology, explore more optimized sampling strategies and algorithms to reduce the errors introduced by the sampling process and improve the calibration effect on the out-of-phase voltage.

4.2.2. Explore new methods to reduce misalignment

Combine emerging material and process technologies, such as new semiconductor materials or advanced nanofabrication processes, to study their impact on the CMOS operational amplifier's misalignment performance, and explore misalignment reduction methods based on these new technologies .

Drawing on techniques and concepts from other fields, such as the potential application of machine learning and artificial intelligence algorithms in circuit optimization, we will study whether the

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distortion of operational amplifiers can be predicted and compensated by intelligent algorithms, and develop innovative distortion reduction strategies.

4.2.3. In-depth Research on the Mechanism of Misalignment

Further study the mechanism of various factors in the CMOS process on the distortion voltage, including a more in-depth analysis of the quantitative relationship between process deviation, temperature variation, device aging and other factors and the distortion voltage. By establishing a more accurate theoretical model, we can provide a more solid theoretical foundation for the optimization of the reduced-distortion technology.

References

[1] *Fu Y, Du C.G., Min R, et al. A low-power low-distortion integrated operational amplifier [J].IC Designs and Applications.2024.(9):851-857.*

[2] *ZHANG Zhou. A three-stage CMOS operational amplifier applied to wideband ADC[N].Journal of Heilongjiang Vocational Institute of Ecological Engineering.2023, 5(Vol.36 No.3).*

[3] *G.Ferri.Low-voltage low-power adaptive biased high-efficiency integrated amplifiers[J].IEEE International Conference on Electronics, Circuit and Systems, 2001.*

[4] *Heung Jeon, Yong-Bin Kim, Minsu Choi.Offset voltage analysis of dynamic latched comparator[C].IEEE 54th International Midwest Symposium on circuits and Systems, 2011.*

[5] *Wang D, Guo GL, Jiang Y, et al. Analysis and design of a rail-to-rail operational amplifier based on chopper technology[C]. Tianjin: Nankai University, 2017.*

[6] *Suntao Wu, Fan Lin, Donghui Guo, et al. Design of CMOS operational amplifiers based on chopper technique for the elimination of out-of-phase voltage [C]. Xiamen: Xiamen University, 2003.*

[7] *Zhang Y.S. The Analysis And Design of Rail-to-Rail Auto-Zero Operational Amplifier [D]. Xiamen: Xiamen University, 2014: 36-40.*

[8] *JIN Xiangliang, CHEN Jie, QIU Yulin. Research on a low-power low-noise correlation dual sampling circuit[J]. Journal of Power and Systems, 2003, 8(3):23-26.*

[9] *L.F. Xu, Research on a CMOS operational amplifier based on digital trimming technique [D]. University of Electronic Science and Technology, 2020:24-25.*

[10] *YIN Wan-jun, BAI Tian-rui.Circuit design og improved folded cascode operational amplifier[C].Chengdu: Southwest Jiao Tong University, 2012.*