Proceedings of the 3rd International Conference on Mechatronics and Smart Systems
DOI: 10.54254/2755-2721/140/2025.21785

The Impact of Chip Development on Engineering Fields: Innovations in Integrated Circuits and Semiconductor Technologies

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Abstract: Advances in chip technology have made modern life possible, and without semiconductor chips, devices such as smartphones, TVs, and computers would not work. The design and manufacture of the chip determine the function and application range of the device. Through continuous innovation and improvement of chip design and manufacturing technology, more functions, higher efficiency, and smaller size devices can be achieved. In these fields, the application of chips and integrated circuits not only improves the performance and function of equipment but also promotes the development of digital society and the application of intelligent technology. This paper explores the critical role of chip technology in various engineering domains, focusing on the advancements in integrated circuits (ICs) and semiconductor materials. It discusses the challenges and developments in chip performance, including response and working speeds, the evolution of RF devices, and the integration of artificial intelligence in chip programming. Artificial intelligence and machine learning technologies are revolutionizing the approach to chip design.

Keywords: Chip Development, Integrated Circuits, Semiconductor Technologies.

1. Introduction

The chip is the core technology of all countries. The integrated circuit is familiar with the variety and capacity. It is an investment that researchers can use from a big field. The chip is the soul of the integrated circuit. The response speed and the working speed are the main problems that can be improved by the development of the chip. Furthermore, the new investment called semiconductors is the development of the chip. The chip can be applied to the program. It is very easy to add a program inside the core with a laptop. Researchers focus on different types of programs of application to show the running speed of the chip. Researchers also test different materials that will affect the integrated circuit on the chip. By using of voltmeter to make sure the integrated circuit is always in the same volt. Researchers also find that different chips work researchers during the integrated circuit starts to work. Researchers are considering what is the major development of the chip. Researchers found out the best chip is made of carbon and should be fireproof because it often runs in a high density of arenas.

The purpose of this paper is to review and study the intelligent chip.

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2. The development of chips influences different engineering fields.

The integrated circuit is the base of electrical engineering. The circuit can be based on the material itself and the chip. The response speed of the chip and the voltage of the integrated circuit are the main functions and abilities. Recent research finds that copper alloy is a reliable material for circuits. It has very great flow ability and is easy to produce. The BCD process has been developed to a smaller size and adopts multi-layer metal structures. This greatly reduces the on-resistance of the power device, thus increasing the current density and efficiency [1][2]. At the same time, the integration degree of the CMOS circuit is increased. The increased integration reduces the negative effects of temperature, pressure, diffusion, and potential gradients when the components of the SPIC circuit are integrated together. On the other hand, the integration complexity of SPIC has been unprecedented, especially the rapid development in recent years, shortening the gap between the development of BCD and pure CMOS processes from other descriptions of BCD theory. The disadvantage of the off-line BCD process is that the no-load voltage at the source end is only a few tens of V. SOI technology can overcome this limitation [3]. So far, due to technical and market reasons, the development of offline BCD technology in reducing the minimum lithography size and increasing the complexity is very limited [4]. It is generally believed that an important factor in judging that a process is developing forward is that its process cost and application value need to be compromised. This does not yet appear in offline B CD[5].In recent years, the rapid development of wireless products has promoted the rapid development of cost-effective RF devices. Compound semiconductors (GaAs, GaN, InGaP, etc.), because of their high cut-off frequency, high voltage resistance, high power density, and high efficiency, it is widely used in RF power devices. So far, GaAs is used to implement RF power amplifiers

3. PA mainstream

Although GaAs have excellent performance, their high cost, inherent high cutoff current, and poor compatibility with analog and digital modules (reduced integrability) have also limited their development. For these reasons, RFLDMOS is an alternative to wireless power amplifiers below 3GHz. In 2004, Philips introduced the fifth-generation RF LDMOS device, enabling WCDMA base station manufacturers to break through the 30% efficiency bottleneck of the RF power amplifier output stage. Developing a program system to build a better chip is more. Because the long-time high-temperature push trap process in the traditional DMOS fabrication process is incompatible with the VLSI process with reduced feature size and the thin gate oxygen layer requiring low defects, especially non-volatile memory devices, the typical gate oxygen thickness is less than 8 nm. In SPI communication mode, one of the SPI communication parties is the primary device [6]. Establishing data communication is currently the most studied.

The research and development results produced by this subject are a set of artificial intelligence programming toolchains for domestic intelligent chips. High-performance operator library, etc. The special programming language developed in the field of intelligent chips can support the programming of intelligent chips using an intelligent instruction set of China's independent intellectual property rights.

The domestic intelligent chip compiler can realize the translation of the special programming language in the field of intelligent computing to the intelligent instruction set of China's independent intellectual property rights and can compile the high-level programming language into domestic intelligence. Can run the assembly language on the chip, and can compile the program written in the high-level programming language into the executable code on the intelligent computing system, in line with the index requirements. Can run the assembly language on the chip, and can compile the program written in the high-level programming language into the executable code on the intelligent

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computing system, in line with the index requirements. The advantages of SOI are obvious [7]. The full dielectric separation between the devices completely inhibits the substrate current, eliminates the latching effect, and improves the strength, for example, suppressing the occurrence of load shedding and ground loss in automotive applications. At the same time, the reduction of substrate parasitic capacitance reduces crosstalk, improves switching speed, and makes low-voltage design possible, which greatly simplifies the design. All-dielectric isolation greatly reduces the loss of silicon wafer area and improves the packaging density. SOI also has superior electromagnetic compatibility (EMC). Consider that traditional CMP systems and polishing pads are available [8].

4. The key technologies in connected multilayer wiring

One of the key technologies in connected multilayer wiring is electrochemical. Electrochemical deposition ECD or electroplating. Although it can be Electroplating through technological improvements. The product process has a Bottom-up filling along the groove side wall. However, studies have found that this filling mechanism is unique. Only fine deep holes and grooves with a large depth-to-width ratio are effective against graphic ruler structures with a large inch and a small aspect ratio does not work and still produce a preserved shape.

The CMP flattening process removes excess copper from each layer due to copper plating Art produced by the excess copper step height is larger and will inevitably be on the subsequent Flat chemical process and even IC manufacturing process efficiency cost and IC The quality and performance of the device have a significant impact Recently, NuTool Company in the United States proposed a new flattening technology - Electrochemical mechanical deposition (Electrochemical mechanical deposition) deposition ECMD technology refers to traditional electrochemical copper deposition

On the basis of the process, non-conductor porous polishing is added between the two electrodes. The pad uses the interference effect of the polishing pad to achieve selective electrochemical copper deposition. The mechanical friction and polishing action of the pad can remove the top Excess copper deposits are thus double removed by selective deposition and mechanical removal The heavy action reduces the thickness of excess copper to achieve the purpose of flattening.

5. Deep learning models adapted to intelligent terminals

The development of high-performance deep learning models adapted to intelligent terminals and the development of domestic AI chip software based on high-performance deep learning networks help 360's IoT products.

Head, 360 smart doorbells, 360 tachographs, and 360 home security brains enable intelligent + security characteristics, serving more than 36 billion user groups. Applied for 3 invention patents. In recent years, the rapid development of wireless products has promoted the rapid development of cost-effective RF devices. Compound semiconductors (GaAs, GaN, InGaP, etc.), because of their high cut-off frequency, high voltage resistance, high power density, and high efficiency, it is widely used in RF power devices[9][10]. So far, GaAs have been used to implement RF power amplifiers. Although GaAs have excellent performance, their high cost, inherent high cutoff current, and poor compatibility with analog and digital modules (reduced integrability) have also limited their development. For these reasons, RFLDMOS is an alternative to wireless power amplifiers below 3GHz. In 2004, Philips introduced the fifth-generation RF LDMOS device, enabling WCDMA base station manufacturers to break through.

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6. Mechanical polishing (Fixed abrasives CMP FA-CMP) technology

Mechanical polishing (Fixed abrasives CMP FA-CMP) technology is Submicron or nanoscale abrasives (such as Al2O3) are bonded with resin SiO2 CeO2, etc.) condense into clusters to form a cylindrical hemispherical shape

Small abrasive blocks of three-dimensional structure with specific shapes such as conical and pyramidal (Size of about tens to hundreds of microns high about tens of microns) according to Certain formation patterns are uniformly and precisely bonded or inlaid in organic thin A composite structure is formed on the surface of the membrane substrate instead of the traditional polishing pad The free abrasive and polishing pad polishing fluid in the CMP is deionized wat Aqueous solutions containing only the basic chemical components are produced during processing The abrasive blocks of the same structure and size are evenly spaced according to certain spatial intervals

It is evenly distributed on the surface of the polishing pad to facilitate the transportation and processing of the polishing liquid The elimination of products is more important is the uniform thickness of the back surface of the polishing pad The organic film substrate is laid flat on a work surface with high precision The abrasive blocks show strong position rigidity in the CMP process Some studies have shown that FA-CMP has the following advantages due to its adoption.

CMP technology combines chemical and physical methods to smooth the surface of the substrate, through a certain pressure and the presence of polishing liquid, the wafer and polishing pad do relative movement, with the organic combination between the mechanical grinding of nano abrasive and the chemical corrosion of oxidants, catalysts, etc., the substance is removed from the wafer surface layer by layer, so as to achieve a high degree of flatness.

Compared with traditional methods, CMP technology uses the "soft wear hard" principle in wear, that is, the softer material is polished to achieve high quality surface polishing, avoiding the surface damage caused by simple mechanical polishing and the shortcomings of slow polishing speed, surface smoothness and poor polishing consistency caused by simple chemical polishing.

7. Future directions for research and development in integrated circuits and semiconductor technologies.

Integrated circuit technology has entered the post-Moore era, how to improve the computing power of chips according to Moore's law through integrated circuit design, new materials and device subversive innovation, is a major technology trend in the post-Moore era. In addition, the chip computing power is evolving from general computing power to special computing power, and the innovation of the architecture is gradually changing from general optimization to special innovation. Through the development of chip technology to meet the special application scenarios (such as near-zero power circuit design, approximate computing, reconfigurable computing, analog computing, heterogeneous computing, etc.), the computing power is greatly improved.

Facing the trend of diversification and specialization of future chip applications, in the post-Moore era, integrated circuit chip technology will gradually develop from the traditional von Neumann paradigm to a new chip with high computing power, high density, low cost, low power consumption and multi-function integration through collaborative optimization innovation of devices, processes and architectures. In addition, due to the strong regulatory ability and integration potential of optoelectronic integrated chips in the optical domain, in future applications, optoelectronic integrated chips that achieve high-speed data transmission and processing will also be an important development direction of integrated circuits.

The semiconductor industry needs to constantly innovate and develop more efficient and energy-efficient materials, which will have a huge impact on the future of the semiconductor industry.

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8. Conclusion

This paper studies the influence of chip development on different engineering fields. This study describes the opportunities and challenges facing development. These advancements and future directions highlight the continuous evolution of chip technology and its profound impact on various engineering fields, driving innovation and sustainability in semiconductor manufacturing.

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