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A Two-Stage Amplifier for Power-Fluctuation-Tolerant Portable Pulse Oximeters

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Abstract: The pulse oximeter is a medical device that utilizes photoplethysmography (PPG) technology to measure blood oxygen saturation (SpO2) in the human body. One of its critical electronic components is the Operational Transconductance Amplifier (OTA). With the increasing demand for higher precision and improved noise immunity in medical instruments, medical-grade integrated circuits are striving for enhanced performance. Complementary Metal-Oxide-Semiconductor (CMOS) technology, as the dominant process in integrated circuit manufacturing, plays a pivotal role in the sampling, amplification, and filtering of biological signals. It is widely applied in the design of various medical device chips. This paper presents the design of a two-stage amplifier for pulse oximeters that operate under power supply fluctuations, utilizing 0.18μm CMOS technology and designed with Cadence software. It achieves high gain and high slew rate while maintaining strong tolerance to power supply voltage fluctuations, ensuring stable performance in the oximeter. The simulation results demonstrate that under a 1.8V power supply, the amplifier designed in this paper exhibits a differential-mode gain of 83.9dB, a unity-gain bandwidth of 54.4MHz, and a common-mode rejection ratio (CMRR) of 83.6dB. Additionally, it achieves a slew rate of 42.6V/μs, with a power consumption of 0.965mW. The low-frequency noise is measured at 4.29μV/sqrt (Hz), and the power supply rejection ratio (PSRR) reaches 97.1dB. These results indicate that the amplifier possesses excellent tolerance to power supply fluctuations.

Keywords: oximeter, amplifier, power supply, high gain, high PSRR

1. Introduction

Portable pulse oximeters are characterized by their compact and lightweight design, enabling rapid measurement of blood oxygen saturation levels [1]. These devices are typically powered by batteries, which experience voltage drops over extended periods of use [2]. This voltage fluctuation can degrade measurement accuracy, necessitating a trade-off between performance and power consumption in the design process, which ultimately limits measurement precision [3]. In pulse oximeters, amplifiers play a crucial role in signal amplification and filtering. The electrical signals acquired through photoplethysmography (PPG) technology are inherently weak and require amplification for further processing and analysis. Additionally, amplifiers, in conjunction with RC networks, form low-pass filters to suppress high-frequency noise and extract clean low-frequency signals. Furthermore, amplifiers are integral components of bandgap reference circuits, providing stable biasing for processing circuits [4]. The stability of the amplifier directly affects the accuracy and reliability of pulse oximeter measurements. This paper delineates the design of an amplifier that

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not only satisfies fundamental performance criteria but also demonstrates a high Power Supply Rejection Ratio (PSRR), thereby ensuring stable operation amidst voltage fluctuations in portable pulse oximeters. The paper is organized into three sections. The initial section examines the impact of voltage fluctuations on the amplifier, encompassing alterations in the MOSFET operating points and delays in circuit response. The second section involves the quantitative calculation and analysis to design the main structure of the circuit, with specific improvements made to enhance voltage fluctuation tolerance. The final section presents simulation results to validate the proposed amplifier's superior performance under varying power supply conditions.

2. Impact of Voltage Fluctuations

The stability of power supply plays a crucial role in determining the overall performance of the amplifier. Fluctuations in the power supply voltage can be amplified by the circuit, leading to decreased output signal accuracy. The impact of the fluctuation on amplifiers is primarily reflected in two aspects: MOSFET operating points and circuit response speed.

2.1. MOSFET Operating Points

The Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is a voltage-controlled device that regulates the current between the drain and source terminals by adjusting the gate voltage. For long-channel MOSFETs, where velocity saturation effects are negligible, the device operates in three distinct regions: the cutoff region, the linear (or triode) region, and the saturation region. Under suitable biasing conditions, the gate voltage is adjusted to ensure that the MOSFET operates within the saturation region, wherein it exhibits a high drain current. In this region, the drain current is controlled by V_{gs}. This characteristic enables MOSFETs to function as amplification elements, allowing the amplifier to achieve the desired gain.

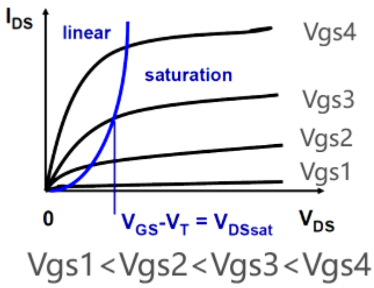

Figure 1: I_D-V_{DS} relationship of an NMOS under different V_{GS}[5]

As shown in Figure 1, both the V_{gs} and the V_{ds} influence the I_{ds}. Variations in supply voltage change V_{ds} and alter the biasing conditions of MOSFET, resulting in changes of operating points. These changes affect key parameters such as transconductance g_m, threshold voltage V_{th}, and output resistance R_o, leading to deviations in gain and bandwidth.

2.2. Circuit Response Speed

The oximeter rapidly and continuously acquires blood oxygen signals, which are then amplified via dedicated amplifiers and processed by subsequent components to derive the subject's blood oxygen information. To improve the resolution of the acquired signals, it is necessary to reduce the signal sampling period to increase the number of sampling points, with the sampling period being

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contingent upon the speed of signal processing [6]. Therefore, the response speed of the amplifier determines the oximeter's processing speed and accuracy for the input signals.

Slew rate (SR) refers to the rate of the output voltage's change in the amplifier. It serves as a measure of the amplifier's ability to respond to rapidly changing input signals. Unfortunately, voltage fluctuations influence the charging and discharging behavior of internal capacitive nodes, thereby affecting the amplifier’s transient response. Increased delay in signal processing may result in phase shifts, reduced SR, and degraded overall performance.

3. Circuit Design

The amplifier circuit in this paper consists of three parts as shown in Figure 2. Section A, B and C represent input circuits, output circuit and biasing circuit, respectively. During the design process, improvements were made to address the impact of power supply fluctuations on the MOSFET's operating points and response speed.

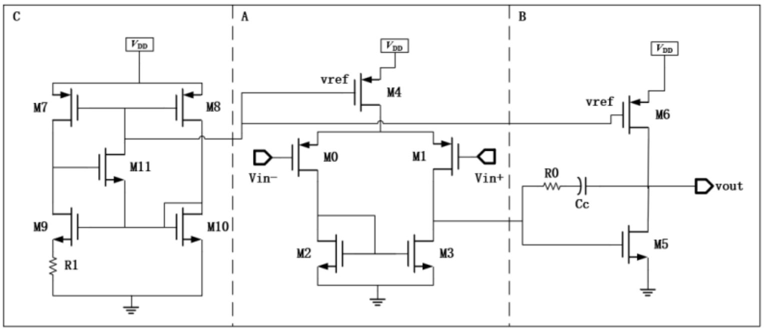

Figure 2: Circuit Diagram

3.1. Input Circuit Design

The differential amplifier amplifies the input differential signals and rejects common-mode signals. It offers strong anti-interference capability, with advantages such as low drift and easy direct coupling between stages [3]. Therefore, in this design, a PMOS differential pair with an active load differential pair is used for the input stage. To enhance the circuit's ability to resist power supply fluctuations, each path of the input stage uses only three MOSFETs, ensuring sufficient voltage headroom to maintain the MOSFETs in the saturation region, thereby maintaining a high gain even during power supply fluctuations, and enabling the amplification of the input blood oxygen signal.

As shown in section A of Figure 2, v_{in-} and v_{in+} represent the differential input signals, while M0 and M1 form the PMOS differential pair, providing a wide input voltage swing. M2 and M3 are current mirror which sever as active loads, and M4 serves as the bias transistor, with its gate connected to the biasing circuit to provide a constant bias current. V_{ref} is generated by the biasing circuit.

The SR is determined by the current available to charge or discharge the output/Miller compensation capacitor, which is mainly governed by the input stage:

$$SR = \frac{I_{d4}}{C_c} \tag{1}$$

Consequently, it is imperative to augment the current of the input stage whilst simultaneously minimizing the Miller capacitance. Furthermore, the gain of this circuit is governed by the equivalent transconductance of the input differential pair, in conjunction with the equivalent impedance of M1 and M3:

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$$A_{v1} = g_{m0,1} * r_{o1}||r_{o3} \tag{2}$$

Consequently, it is essential to enhance the g_m M0 and M1, while also increasing the r_o of the input transistor M1 and the active load M3. To this end, the bias current I_{d4} for the input stage is set at 60μA, with M0 and M1 allocated an overdrive voltage of 160mV, and M2 and M3 allocated an overdrive voltage of 110 mV. To bolster the common-mode rejection capability of the circuit, M0 and M1, as well as M2 and M3, are designed with identical dimensions. When the MOSFETs operate in the saturation region, they follow the square-law formula:

$$I_d = \frac{1}{2} u_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \tag{3}$$

$$g_m = \frac{2I_d}{V_{GS} - V_{TH}} \tag{4}$$

$$r_o = \frac{1}{\lambda I_d} \tag{5}$$

Based on equations (1), (2), (3), (4) and (5), the parameters of the input transistors and the load transistors can be calculated.

3.2. Output Circuit Design

The output stage provides high gain and high voltage swing while converting the differential input into a single-ended output. In this paper, a common-source configuration is adopted for the output stage, which achieves high gain with fewer MOSFETs, offers rail-to-rail output, and provides a larger voltage headroom, thereby enhancing the circuit's immunity to power supply fluctuations [7].

As shown in section B of Figure 2, M5 serves as the amplification transistor, providing voltage gain, while M6 functions as the current-source load transistor. The reference voltage v_{ref} is generated by the biasing circuit.

The differential gain of the output stage satisfies:

$$A_{v2} = g_{m5} \left(r_{o5} // r_{o6} \right) \tag{6}$$

Since the gate of M5 is connected to the drain of M3, in order to ensure that M5 operates in the saturation region to achieve the maximum gain, it is necessary to set the overdrive voltages of M2, M3, and M5 to the same value. In this paper, a 110mV overdrive voltage is allocated.

In this paper, the Miller compensation technique is employed to achieve the separation of the dominant and non-dominant poles, thereby altering the PM and enhancing the stability of the circuit. The capacitor C_c in section B of Figure 2 represents the Miller compensation capacitor, which primarily influences the GBW and the PM:

$$GBW = \frac{g_{m1}}{2\Pi C_c} \tag{7}$$

From equations (1) and (7), it is evident that a smaller Miller compensation capacitance allows for achieving both a larger SR and a higher GBW. Therefore, in this paper, C_c = 0.6pF is chosen. To ensure a phase margin of 60° for enhanced circuit stability, the non-dominant pole is controlled to be at three times the GBW [8].

$$P_2 \approx \frac{g_{m6}}{C_L} \tag{8}$$

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Since the non-dominant pole satisfies equation (8), and combining this with equation (4), we can select I_{d5} = 450μA. Parameters of M5 can then be preliminarily determined based on equations (3) and (4).

The Miller compensation capacitor C_c introduces a right-half-plane zero in the frequency domain. To maintain sufficient PM, a nulling resistor R_0 is introduced in section B of Figure 2 to control the position of the zero. This resistor shifts the zero to higher frequencies, ensuring the circuit has enough PM and improving stability.

3.3. Biasing Circuit Design

In the input and output circuit designs, we have not yet provided the method for determining the dimensions of the bias transistors M4 and M6, which is due to the design of the biasing circuit in this paper.

The biasing circuit provides bias currents to the two-stage amplifier circuit. In an ideal scenario, it consumes low power and is unaffected by fluctuations in the power supply voltage [9]. This study utilizes a cascode current mirror incorporating resistor-induced mismatch as the biasing circuitry. The resultant reference current remains unaffected by variations in the power supply voltage, thereby significantly augmenting the amplifier's immunity to power supply fluctuations. A simple four-transistor cascode biasing circuit is utilized in this paper to ensure that all MOSFETs operate in the saturation region while minimizing circuit area and power consumption.

In section C of Figure 2, M7, M8, M9, and M10 form the basic cascode biasing circuit. Since M7 and M10 function as MOS-diode loads, I_{d7} , I_{d8} and V_{ref} are relatively independent of V_{dd}. The voltage relationship between M9 and M10, as expressed in equation (9), leads to the same conclusion, which shows that the biasing circuit generates an "ideal" bias current that is independent of the power supply voltage. This circuit is biased by its own mismatch resistor R_1, and by adjusting the value of resistance, currents with arbitrary temperature coefficients can be generated. Importantly, this current is independent of the supply voltage. The specific resistance values are determined by the chosen reference current.

$$\left(\frac{2I_{d7}}{u_n C_o x\left(\frac{W_N}{L_N}\right)}\right)^{\left(\frac{1}{2}\right)} + V_{TH9} + I_{d7}R_1 = \left(\frac{2I_{d8}}{u_n C_o x\left(\frac{W_N}{L_N}\right)}\right)^{\left(\frac{1}{2}\right)} + V_{TH10} \tag{9}$$

Transistors M7 and M8 within the biasing circuit, in conjunction with M4 from the input circuit and M6 from the output circuit, collectively constitute a cascode current mirror configuration, thereby fulfilling the biasing function for the two-stage amplifier. The reference current is set to 15μA, and the overdrive voltage of M7 is selected to be 180mV. Based on the bias currents chosen for the input and output circuits, the parameters of the biasing transistors can be calculated using equations (3) and (4). Using the established reference current and equation (9), the relevant parameters of MOSFETs and resistors are obtained through simulation verification.

The simple biasing circuit addresses the issue of power supply fluctuations affecting the bias current, ensuring that the MOSFETs can operate normally [10]. Unfortunately, since the bias circuit is provided by a cascode current mirror, with MOSFETs connected in a MOS-diode configuration, fluctuations in the supply voltage, especially a reduction in voltage, cause a decrease in the SR of the amplification circuit, which impacts the circuit's fast response performance. To tackle this challenge, this paper introduces a startup circuit design. By sampling the operational state of the cascode unit, this circuit responds only when the circuit is "started." In section C of Figure 2, M11 serves as a simple start-up element, extracting current from the MOS-diode device (M7) to increase the slew rate [11], thereby improving the circuit's fast response capability.

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Table 1: Parameters of transistors for amplifier

Devices	M0, M1	M2, M3	M4	M5	M6	M7, M8	M9	M10	M11
W/L(um/um)	21/0.8	20/1.4	81/2	324/1.4	700/2	24/2	20/2	5/2	0.18/2

Table 2: Parameters of capacitor and resistance

Devices	C_C(pF)	$R_0(\Omega)$	$R_1(\Omega)$
Parameters	0.6	320	12k

In the simulation design, to meet the high gain, high power supply rejection ratio, and high slew rate requirements for the oximeter's operational amplifier, a trade-off design was made in conjunction with other parameters. The final device parameters are summarized in Table 1 and Table 2.

4. Simulation Results

The amplifier in this study is simulated and verified using the Spectre simulator within the Cadence software. The simulation tests for various performance parameters are conducted under the following conditions: an ambient temperature of 25°C, a supply voltage of 1.8V, an input common-mode voltage of 0.9 V, and a load capacitance of 2pF.

Figure 3 presents the frequency response simulation results of the amplifier. The first curve in the graph represents the gain curve (dB20), where the open-loop gain at low frequencies is 83.9096dB. Due to the presence of the dominant pole, the gain decreases at a rate of 20dB per decade as the frequency increases, reaching unity gain at a frequency of 54.44MHz. The second curve depicts the phase curve. Given the relatively low frequency of the dominant pole and the existence of a zero in the circuit, the phase initially shifts by approximately 45° as the frequency approaches the dominant pole. Subsequently, as the frequency nears the zero, the pole-zero cancellation occurs, stabilizing the phase momentarily before it continues to decrease. The implementation of Miller compensation in this design effectively separates the dominant and secondary poles, resulting in a phase margin of 62.901° at the unity-gain frequency (54.44 MHz), thereby ensuring stability of the circuit.

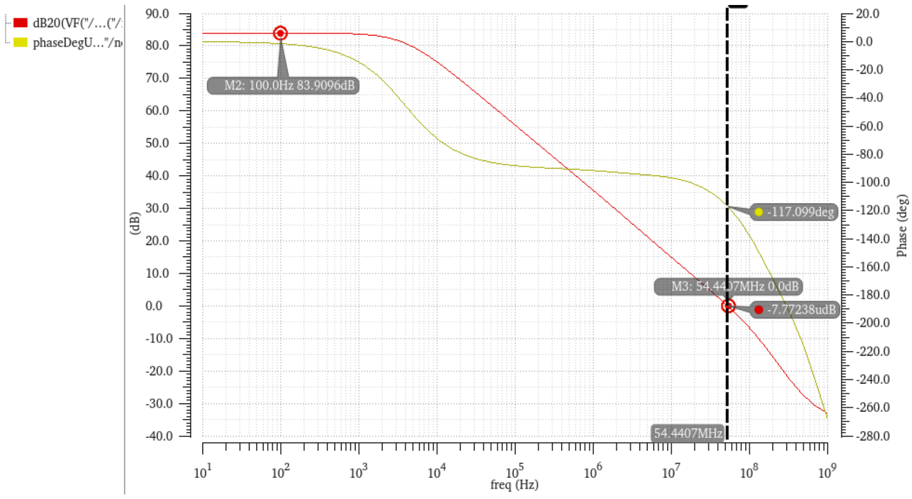

Figure 3: Measured voltage-frequency relationship of amplifier

Fig. 4 shows the simulation results for the PSRR. At low frequencies, the PSRR maintains a relatively high value. However, as the frequency increases, the PSRR exhibits a declining trend. The negative power supply rejection ratio (PSRR-) is 97.0773dB, and the positive power supply rejection

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ratio (PSRR+) is 95.708dB. These results indicate that the amplifier designed in this paper possesses strong resistance to power supply interference.

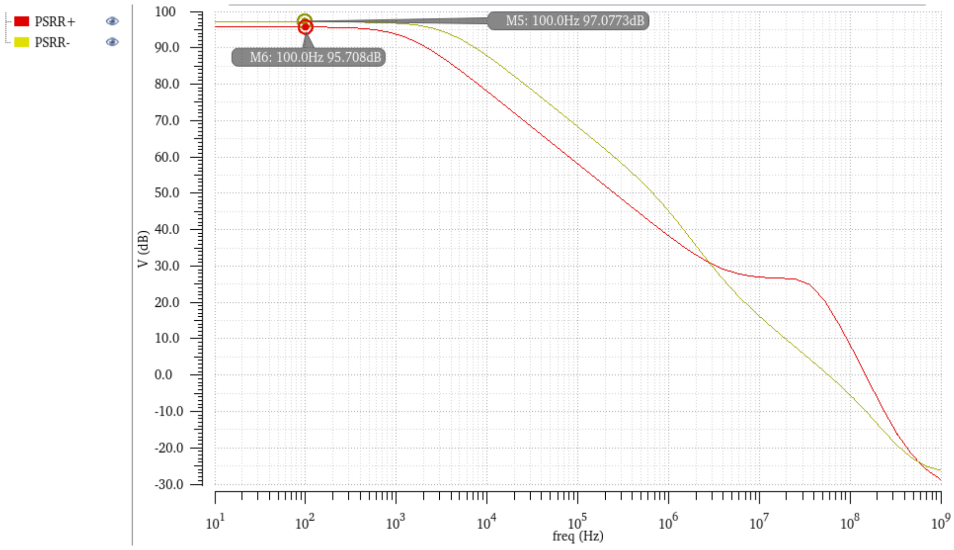

Figure 4: Measured PSRR-frequency relationship of amplifier

Figure 5 illustrates the slew rate simulation results. As shown in the figure, the output node exhibits a faster response speed during pull-down compared to pull-up. The measured slew rate is 40.0V/µs. These results demonstrate that the operational amplifier design in this study successfully mitigates the impact of power supply voltage fluctuations and achieves a rapid response speed.

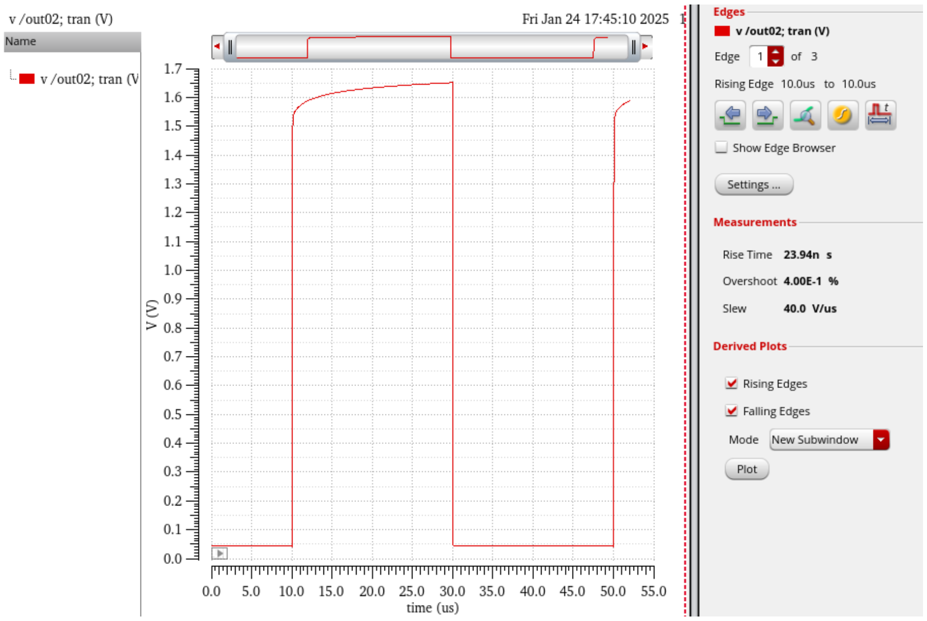

Figure 5: Measured voltage-time (SR) relationship of amplifier

Table 3 presents the simulated characteristics of the amplifier. As shown in Table 3, the amplifier demonstrates significant advantages in parameters such as gain, PSRR, slew rate, and CMRR.

Table 3: Simulated characteristics of amplifier

Parameter	Gain (db)	PM (°)	GBW (MHz)	PSRR- (db)	CMRR (db)	Power (mW)	Noise (uV/sqrt(Hz))	SR (V/us)
Results	83.91	62.9	54.44	97.08	83.59	0.965	4.29	40.0

5. Conclusions

This paper presents the design of a two-stage amplifier for use in blood oximeters subjected to power supply fluctuations. The amplifier exhibits excellent performance with high gain, high PSRR, and high SR, showing strong resistance to power supply voltage fluctuations. The input circuit utilizes a PMOS differential pair with an active load differential pair, effectively suppressing common-mode signals while enhancing the circuit's immunity to power supply variations. The output circuit employs a common-source configuration, providing DC gain along with rail-to-rail output. The biasing circuit incorporates a cascode current mirror employing offset-induced resistors, whose characteristics exhibit independence from the power supply voltage. This design effectively augments the amplifier's immunity to power supply fluctuations, thereby ensuring a stable DC bias. Under a 1.8V supply voltage and a 2pF load capacitance, the designed amplifier achieves a differential gain of 83.9dB, a GBW of 54.4MHz, a CMRR of 83.6dB, a slew rate of 42.6V/µs, a circuit power consumption of 0.965mW, low-frequency noise of 4.29µV/sqrt (Hz), and a PSRR of 97.1dB. Although there is room for improvement in low-frequency noise, the amplifier designed in this paper already offers significant performance advantages, particularly in terms of its resistance to power supply fluctuations.

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