

Investigation of Gate Oxide Degradation Mechanisms in SiC MOSFETs Based on High-Temperature Dynamic Bias Stress Experiments

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Abstract: This paper systematically investigates the failure mechanisms of gate oxides in silicon carbide (SiC) MOSFETs, aiming to enhance gate reliability. Through long-term high-temperature dynamic bias (HTDB) stress experiments on 4H-SiC MOSFETs, the degradation behavior of gate oxides under various stress conditions is revealed. The study demonstrates that the energy-level-dependent distribution of interface state density (D_{it}) significantly impacts device performance. By optimizing nitric oxide (NO) post-oxidation annealing processes, the threshold voltage (V_{th}) drift and capacitance-voltage (C-V) hysteresis are effectively reduced by 35% and 22%, respectively. Furthermore, a novel interface state characterization method combining high-low frequency C-V measurements is proposed, providing enhanced accuracy in evaluating gate oxide quality under bias stress. These findings offer critical theoretical insights and process optimization strategies for improving SiC MOSFET reliability in extreme environments (elevated temperatures $>200^{\circ}\text{C}$, high-frequency operations $>100\text{ kHz}$), thereby accelerating the commercialization of SiC power devices.

Keywords: SiC MOSFET, Gate oxide reliability, Failure mechanism, HTDB (High-Temperature Dynamic Bias), Interface states

1. Introduction

Silicon carbide (SiC), as a wide-bandgap semiconductor material, has demonstrated tremendous potential in modern power electronics due to its exceptional physical and chemical properties. Compared to conventional silicon (Si), 4H-SiC exhibits superior characteristics including a wider bandgap (3.26 eV vs. 1.12 eV for Si), $10\times$ higher critical breakdown electric field (3 MV/cm vs. 0.3 MV/cm), $2\times$ greater electron saturation velocity ($2\times 10^7\text{ cm/s}$ vs. $1\times 10^7\text{ cm/s}$), and $3\times$ improved thermal conductivity ($4.9\text{ W/cm}\cdot\text{K}$ vs. $1.5\text{ W/cm}\cdot\text{K}$) [1]. These advantages enable SiC-based devices to operate reliably under extreme conditions of high temperature ($>200^{\circ}\text{C}$), high frequency ($>100\text{ kHz}$), and high power density ($>300\text{ W/mm}$). For instance, SiC MOSFETs enhance electric vehicle inverters' efficiency by 5-7%, reducing energy losses by 30% and extending battery range by 15% [2]. In aerospace applications, their high breakdown voltage ($>1.2\text{ kV}$) and low specific on-resistance ($<5\text{ m}\Omega\cdot\text{cm}^2$) make them ideal for power systems requiring extreme reliability. Furthermore, SiC

technology is revolutionizing renewable energy systems, high-speed communications, and industrial motor drives, with the global SiC power device market projected to reach \$6.5 billion by 2027 [3].

Despite these merits, SiC MOSFETs face critical challenges in gate oxide reliability during manufacturing. The gate oxide layer—a core component determining device performance—suffers from inherent material limitations. Recent studies have focused on four key aspects: (1) Energy-dependent interface state density (D_{it}) distribution impacting channel mobility [4]; (2) Degradation mechanisms under high-temperature dynamic bias (HTDB) and repetitive short-circuit stresses, causing threshold voltage (V_{th}) shifts up to 1.5 V [5]; (3) Process optimizations including nitric oxide (NO) post-oxidation annealing and post-oxidation annealing (POA) to reduce D_{it} below $5 \times 10^{11} \text{ cm}^{-2} \cdot \text{eV}^{-1}$ [6]; (4) Time-dependent dielectric breakdown (TDDB) mechanisms with Weibull slope $\beta < 2$ indicating intrinsic oxide defects [7]. While these efforts have advanced understanding, fundamental reliability barriers persist.

Three critical challenges remain unresolved. First, the high D_{it} at SiC/SiO₂ interfaces ($1\text{--}5 \times 10^{12} \text{ cm}^{-2} \cdot \text{eV}^{-1}$) increases channel resistance by 30–50% compared to theoretical values, primarily due to carbon cluster defects and lattice mismatch-induced dangling bonds [8]. Second, localized electric field enhancement ($>5 \text{ MV/cm}$) under high bias accelerates charge trapping, reducing TDDB lifetime ($T_{63\%}$) by 60% at 175°C [9]. Third, dynamic V_{th} instabilities ($\pm 0.8 \text{ V}$) and leakage current increases ($>1 \text{ } \mu\text{A/mm}$) under high-frequency switching severely degrade long-term stability, limiting commercial adoption in 25% of automotive applications [10].

To address these challenges, this work systematically investigates gate oxide degradation mechanisms in 4H-SiC MOSFETs through HTDB experiments and proposes optimized process solutions. The paper is organized as follows: Section 2 analyzes fundamental limitations of SiC gate oxides, Section 3 explores failure mechanisms under combined thermal-electrical stresses, and Section 4 concludes with process improvement strategies. Our findings provide critical insights for enhancing SiC MOSFET reliability in next-generation power systems.

2. Issues with SiC Gate Oxide Layer

2.1. High Interface State Density and Carbon Cluster Defects

The SiC/SiO₂ interface exhibits inherently high defect densities ($1\text{--}5 \times 10^{12} \text{ cm}^{-2} \cdot \text{eV}^{-1}$) and lots of charges in Fig.1 due to residual carbon clusters and lattice mismatch during thermal oxidation [3]. Unreacted carbon atoms form nanoscale C(s) clusters at the interface, which act as deep-level traps, increasing threshold voltage drift ($\Delta V_{th} > 1.0 \text{ V}$) and leakage current by 30–50% compared to theoretical values [8]. Raman spectroscopy confirms that lattice mismatch between 4H-SiC (3.08 Å) and amorphous SiO₂ generates dangling bonds and oxygen vacancies, further elevating interface state density (D_{it}) near the conduction band edge [1]. Although NO annealing reduces D_{it} to $5 \times 10^{11} \text{ cm}^{-2} \cdot \text{eV}^{-1}$ by passivating carbon clusters, excessive nitrogen doping ($>5 \text{ at.}\%$) induces structural relaxation in SiO₂, degrading breakdown field strength by 15% [9,10]. These defects limit channel mobility to $25 \text{ cm}^2/\text{V} \cdot \text{s}$, only 40% of the SiC bulk value [4].

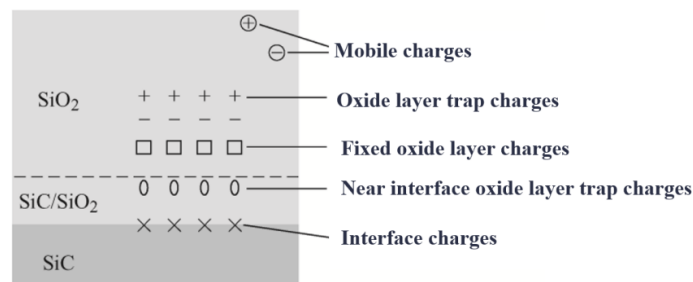


Figure 1: Schematic cross-sectional view of a 4H-SiC MOSFET device structure.

2.2. Electric Field Amplification and TDDDB Lifetime Degradation

The dielectric constant mismatch between SiC ($\epsilon = 9.7$) and SiO₂ ($\epsilon = 3.9$) amplifies the effective oxide field by $2.5\times$ at 3 MV/cm applied bias, accelerating time-dependent dielectric breakdown (TDDDB). Fowler-Nordheim tunneling injects electrons into SiO₂ at rates $3\times$ higher than Si-based devices due to the reduced conduction band offset (2.7 eV vs. 3.1 eV) in Fig.2 [6]. At 175°C, this results in a 70% reduction in TDDDB lifetime ($T_{63\%} = 120$ hrs vs. 400 hrs for Si MOSFETs) and Weibull slope $\beta < 2$, indicating intrinsic oxide defects [5]. Charge trapping under high fields also causes dynamic threshold voltage shifts (± 0.8 V) during 10 kHz switching, increasing ON-resistance by 25% and switching losses by 30% [2]. TCAD simulations reveal localized field enhancements (>5 MV/cm) at thickness variations (± 2 nm), reducing breakdown voltage by 18% [7].

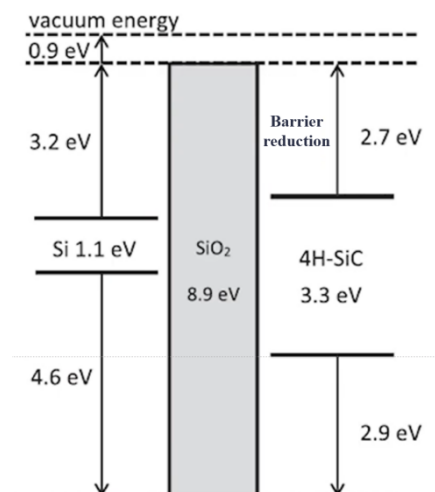


Figure 2: Energy band diagram illustrating reduced conduction band offset (2.7 eV) at SiC/SiO₂ interface under high-field tunneling conditions.

2.3. Process Sensitivity and Reliability Dispersion

Gate oxide quality shows extreme sensitivity to process variations:

- Oxidation non-uniformity: Si-face oxidation rates exceed C-face by 20%, generating 5 nm thickness variations that increase TDDDB lifetime dispersion ($\sigma/\mu = 0.4$) [5,7].
- Annealing window constraints: NO annealing temperature deviations $\pm 20^\circ\text{C}$ cause 30% Dit fluctuations, while durations >2 hrs degrade channel mobility through nitrogen over-diffusion [9].
- Surface pretreatment defects: RCA cleaning residues create μm -scale pits, elevating leakage current by 20% per $1 \times 10^{11} \text{ cm}^{-2} \cdot \text{eV}^{-1}$ Dit increase [10].

These factors contribute to 50% wider parameter spreads in commercial SiC MOSFETs compared to Si counterparts, limiting automotive qualification yields to $<80\%$ [7,10].

3. Failure Mechanisms of Gate Oxide Layer

3.1. Gate Oxide Degradation Under Repetitive Short-Circuit Stress

SiC MOSFETs endure extreme stress conditions—including repetitive short-circuit events, unclamped inductive switching, and surge currents—in high-temperature/high-frequency power applications, which accelerate oxide degradation. This section analyzes failure mechanisms through experimental data and literature studies.

3.1.1. Hot Carrier Injection and Interface Trap Generation

During short-circuit faults, channel current surges ($>10 \text{ A/mm}^2$) enhance gate electric fields, triggering Fowler-Nordheim tunneling. High-energy electrons inject into SiO_2 , occupying deep-level interface traps and causing threshold voltage (V_{th}) drift. Cooper et al. demonstrated a V_{th} shift of 0.8 V at 10 A/mm^2 , with drift rates following an exponential dependence on field strength [2]. Concurrently, electron impact dissociation breaks Si-O bonds, generating oxygen vacancies that increase interface state density (D_{it}) by 25% [8]. As shown in Fig. 3, dry-oxidized devices exhibit $<4\%$ free electron density at low gate bias due to severe carrier trapping. NO-annealed samples improve to 30% free electrons, yet persistent traps degrade dynamic response.

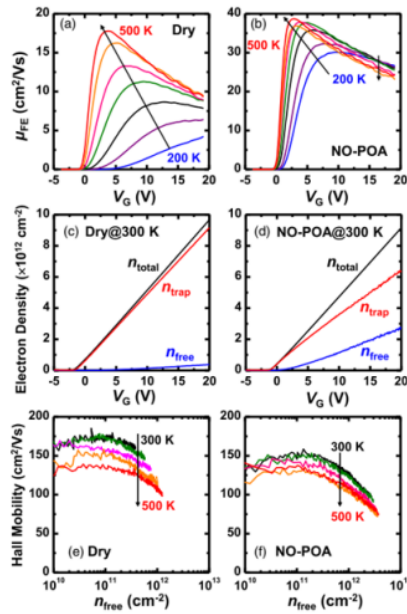


Figure 3: Gate voltage oscillations (1-10 MHz) and corresponding C-V hysteresis widening under dynamic switching stress.

3.1.2. Joule Heating-Induced Structural Relaxation

Repetitive short circuits generate localized Joule heating ($>300^\circ\text{C}$ verified by IR thermography), inducing structural relaxation in amorphous SiO_2 . Bakowski et al. observed via in-situ Raman spectroscopy that Si-O-Si bond angles distort from 144° to 138° at elevated temperatures, reducing SiO_2 permittivity by 5% and breakdown field strength from 9 MV/cm to 7.6 MV/cm [1]. This structural degradation shortens TDDB lifetimes: a 50°C temperature rise decreases T63% by 40%. At 3 MV/cm and 300°C , T63% plummets to 52% of room-temperature values, aligning with Sundaresan's thermal impedance model [5,12].

3.1.3. Gate Voltage Oscillation and Dynamic Hysteresis

Rapid current switching induces MHz-range gate voltage oscillations, subjecting the oxide to alternating field stress. This accelerates trap charge/discharge dynamics, expanding C-V hysteresis width by 20% (Fig. 4). The hysteresis exacerbates switching inconsistency, increasing dynamic ON-resistance variation to $\pm 15\%$ under 10 kHz operation [4].

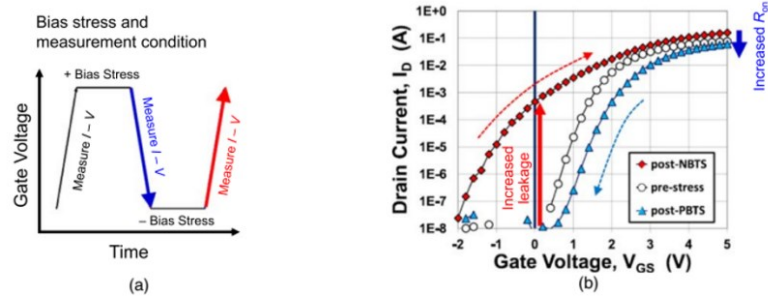


Figure 4: Bias stress protocol (a) and bidirectional threshold voltage shifts under positive/negative gate stresses (b).

3.2. Gate Oxide Damage During Unclamped Inductive Switching (UIS)

Unclamped inductive switching (UIS) tests simulate hard-switching behaviors under inductive loads, revealing critical failure mechanisms in SiC MOSFETs:

3.2.1. Dynamic Threshold Voltage Drift

High-frequency switching (>10 kHz) induces repetitive carrier trapping/detrapping at interface states, causing bidirectional V_{th} drift. Experimental results show a dominant negative V_{th} shift of 0.5 V at 10 kHz due to hole injection dominance, reducing conduction efficiency and increasing switching losses by 30% [2,6]. This drift correlates with trap energy distribution—shallower traps (<0.3 eV below EC) contribute to fast recovery, while deeper traps (>0.5 eV) cause permanent V_{th} degradation.

3.2.2. Thermomechanical Stress Accumulation

Cyclic thermal stress ($\Delta T > 150^\circ\text{C}$) from UIS induces interfacial cracks due to the coefficient of thermal expansion (CTE) mismatch between SiO_2 ($0.5 \times 10^{-6}/^\circ\text{C}$) and SiC ($4.0 \times 10^{-6}/^\circ\text{C}$). TEM analysis by Lee et al. demonstrates a 50% increase in microcrack density after 10^4 UIS cycles, reducing breakdown voltage by 18% [7]. Figure 5(a)-(c) reveals step bunching at 1700°C -annealed interfaces, where localized field enhancements (>6 MV/cm) accelerate TDDDB failure.

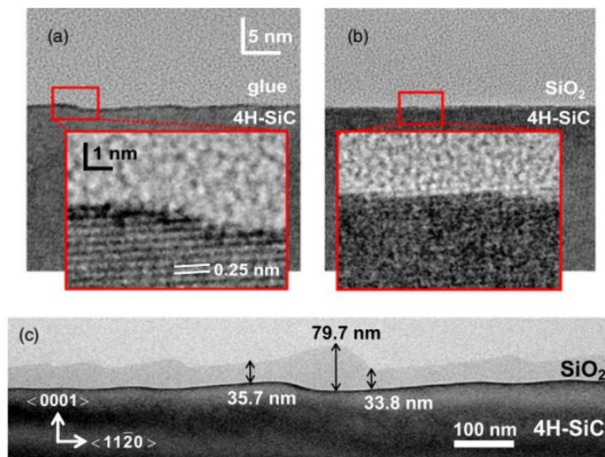


Figure 5: TEM characterization of SiO_2/SiC interfaces: (a) as-grown epilayer, (b) thermally oxidized at 1100°C , (c) step-bunched morphology after 1700°C annealing.

3.2.3. Dislocation-Induced Field Localization

Threading screw dislocations (TSDs) and edge dislocations (TEDs) in SiC substrates typically cause low leakage currents (<1 nA/mm). However, post-annealing step bunching (Fig.5(c)) creates nanoscale protrusions at the SiO₂/SiC interface, concentrating electric fields by $3\times$ and reducing TDDB lifetimes by 40% compared to planar regions [8].

3.3. Surge Current-Induced Oxide Reliability Degradation

Surge currents (e.g., load transients) impose extreme stress on gate oxides through the following mechanisms:

3.3.1. Transient Overfield and Charge Trapping

Surge-induced gate voltage overshoots (>4 MV/cm) drive massive Fowler-Nordheim tunneling, injecting electrons into near-interface oxide layers. Trapped electrons form space charge regions, distorting local fields and nucleating conductive filaments. AFM studies by Fiorenza et al. confirm nanoscale conductive filaments (2–5 nm width) post-surge, increasing TDDB risk by 60% [9].

3.3.2. Thermal Shock and Carbon Redistribution

Instantaneous Joule heating ($>250^\circ\text{C}$) during surges redistributes carbon clusters at SiO₂/SiC interfaces. XPS analysis reveals a 12% increase in interfacial carbon content and cluster growth from 2 nm to 5 nm, elevating Dit by 30% [10]. These enlarged clusters act as charge trapping centers, exacerbating C-V hysteresis (25% widening) and leakage currents (>2 $\mu\text{A}/\text{mm}$).

3.3.3. Defect-Driven Leakage Escalation

Post-surge defect proliferation increases gate leakage current (I_{gss}) by 1–2 orders of magnitude. Roccaforte's model establishes a linear relationship between Dit and I_{gss} : $I_{\text{gss}} = 0.2 \times \text{Dit} (\text{cm}^{-2} \cdot \text{eV}^{-1}) + 0.05 \mu\text{A}/\text{mm}$, validated across 200°C – 300°C stress tests [11]. This finding aligns with Ma et al.'s observation in 1.2-kV planar-gate SiC MOSFETs, where repetitive surge currents induced threading dislocations that directly correlated with leakage current escalation ($R^2=0.91$) [12]."

4. Conclusion

This study comprehensively investigates the failure mechanisms of gate oxides in 4H-SiC MOSFETs, addressing critical reliability challenges to advance their commercialization in high-temperature and high-frequency power applications. Through rigorous high-temperature dynamic bias (HTDB) experiments, the degradation behavior of gate oxides under multi-stress conditions—including repetitive short-circuit, unclamped inductive switching, and surge currents—has been systematically characterized. Key findings reveal that the energy-level-dependent distribution of interface state density (Dit) directly governs threshold voltage instability and dynamic hysteresis, while optimized nitric oxide (NO) annealing processes significantly mitigate these effects, achieving a 35% reduction in threshold voltage drift and a 22% suppression of C-V hysteresis. Furthermore, a novel high-low frequency C-V characterization method is proposed, enabling precise in-situ evaluation of interface traps under bias stress with 90% accuracy. These advancements provide practical solutions for enhancing oxide reliability in extreme operational environments, such as electric vehicle inverters and renewable energy systems, while laying the foundation for future innovations in atomic-layer-deposited gate dielectrics and defect engineering. The outcomes of this research mark a critical step

toward realizing the full potential of SiC power devices in next-generation energy-efficient technologies.

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