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# *Design and Application of High-Efficiency Gallium Nitride (GaN)-Based Power Electronic Devices*

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***Abstract:*** As silicon technology reaches its physical limits, gallium nitride (GaN) electronic devices are emerging as a disruptive solution in power electronics. GaN devices, with their superior breakdown voltage, exceptional thermal stability, and outstanding high-frequency performance, offer considerable benefits over traditional silicon-based devices. And these properties increase power density, switching speed, and greatly enhance energy efficiency, making GaN a key technology driving the development of next-generation power electronic systems. This paper reviews the latest advancements in GaN epitaxial growth, device design, and reliability optimization, while delving into key challenges such as thermal management and dynamic resistance degradation under high-power conditions. The results highlight the critical role of heterojunction engineering and gate structure innovations in suppressing interface defects and enhancing device efficiency. As an emerging technology, GaN power devices, which hold considerable commercial potential, are set to transform power density, switching efficiency, and operational stability in next-generation electronic applications.

***Keywords:*** GaN Devices, High-Frequency Performance, HEMT, Normally-Off Operation

## 1. Introduction

As silicon-based technologies reach their physical limits, gallium nitride (GaN) electronic devices are gaining significant attention due to their exceptional properties, such as high breakdown voltage, excellent thermal conductivity, and high-frequency operational capabilities. In recent years, studies on GaN devices has mainly been directed towards epitaxial growth, device structure optimization, and enhancing reliability. However, efficient thermal management under high-frequency and high-power conditions remains a significant challenge. Despite progress in reducing conduction losses and mitigating interface defects, systematic research on long-term stability prediction methods is still lacking. This paper seeks to explore methods for improving the performance of GaN power devices, with a focus on thermal management and reliability optimization in high-frequency and high-power environments, by advancing material growth techniques, device design, and thermal control strategies. Through an analysis of relevant literature and existing research, it examines how to achieve effective thermal management and long-term reliability for GaN devices under extreme conditions, addressing challenges like overheating and dynamic resistance degradation to enhance the stability and efficiency of GaN devices in practical applications. Thus, the paper may provide a foundation for the widespread adoption of GaN devices, supporting their use in electric vehicles, renewable energy, communications, and consumer electronics, with notable practical implications and development potential.

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## 2. Material properties of GaN and power device design

### 2.1. Physical characteristics and advantages of GaN

Third-generation semiconductor materials, represented by GaN, are known for their wide bandgap characteristics. GaN has a bandgap of 3.4 eV, significantly higher than that of first- and second-generation semiconductors. Its key attributes include an exceptionally high breakdown electric field, high electron drift velocity, excellent junction temperature tolerance, and outstanding mechanical hardness, which enable large-scale device integration. The main performance parameters of GaN, SiC, GaAs, and Si are shown in Table 1 [1].

Table 1: Comparison of key performance metrics for GaN, SiC, GaAs, and si materials

| Performance Parameter | GaN | SiC | GaAs | Si |
|---|---|---|---|---|
| Bandgap energy(eV) | 3.4 | 3.2 | 1.4 | 1.1 |
| Critical breakdown electric field(MV/cm) | 3.3 | 3.5 | 0.4 | 0.3 |
| Electron mobility(cm2/(V*s)) | 2000 | 650 | 8500 | 1500 |
| Saturation drift velocity(*107 cm/s) | 2.5 | 2.0 | 2.0 | 1.0 |
| Thermal conductivity(W/(cm*K)) | 2.2 | 4.9 | 0.54 | 1.5 |

The wide bandgap and high critical breakdown electric field of GaN are instrumental in reducing on-state resistance. In power electronic systems, the carrier transport mechanism in semiconductor devices predominantly manifests as n-type conductivity, where electrons serve as majority carriers. Consequently, electron mobility ($\mu=V/E$) emerges as a pivotal parameter for material evaluation, quantitatively describing the electron drift velocity (V) under an applied electric field (E). Materials with high electron mobility exhibit superior charge transport efficiency in the weak-field regime (Ohmic region), which is a key factor for optimizing high-frequency devices. Besides, the saturation drift velocity represents the ultimate drift velocity limit of carriers under increasing electric fields. Beyond a critical threshold, the carrier velocity shows a nonlinear dependence on the field intensity, eventually approaching a saturation limit [2]. Higher saturation drift velocity thresholds notably extend the operational frequency range of devices. Thermal conductivity, representing the material's heat dissipation ability, is a key factor in assessing its suitability for high-temperature applications. Higher thermal conductivity values indicate enhanced thermal management capabilities, which are essential for operation in high-temperature environments [3].

### 2.2. Working principles of GaN-based power devices

GaN devices mainly consist of GaN transistors and diodes, with GaN transistors further classified into depletion-mode and enhancement-mode types. Enhancement-mode devices are inherently safer for power electronics, as they remain non-conductive at zero gate-source voltage, hence effectively avoiding shoot-through risks during startup or power control. In contrast, depletion-mode devices conduct by default and require negative bias to turn off [4]. The most commercially prevalent GaN devices are heterojunction field-effect transistors (HFETs), also referred to as high electron mobility transistors (HEMTs). HEMTs inherently operate in depletion-mode due to their two-dimensional electron gas (2DEG) channel. To achieve normally-off (enhancement-mode) operation, a depletion-mode GaN HEMT is paired with a low-voltage Si MOSFET in a cascode arrangement [4]. In this configuration, both devices conduct the same channel current when on and block voltage when off [5]. The inherent properties of wide-bandgap semiconductors enable GaN power devices to deliver significant performance improvements. These include a marked reduction in on-resistance to reduce

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conduction losses, lower gate charge and reverse recovery charge that enhance converter efficiency, reduced parasitic capacitance enabling high-frequency switching in compact power electronics, and superior thermal stability that reduces the need for extensive cooling systems.

### 2.3. Difficulties and structural optimization of power devices

GaN-based HEMT technology has transitioned from laboratory research to commercial production, but several key design difficulties remain unresolved. One such issue is current collapse, which refers to the temporary increase in on-resistance and a sharp decrease in output current swing during high-frequency, large-signal operation. This instability is primarily attributed to trap-related charge dynamics. Factors such as temperature, load current, and bus voltage markedly impact this behavior [6]. Optimization strategies typically involve redesigning the field plate structure to redistribute the gate-drain electric field away from the gate edge. Another issue is that voltage oscillations during switching transients can trigger false turn-on events. Additionally, gate breakdown can permanently damage the device. Proper design of the printed circuit board (PCB) layout is vital for minimizing common-mode noise induced by parasitic impedances [4]. In terms of thermal management, the reduced dimensions of GaN power devices heighten the associated thermal challenges [7]. Surface-mount devices (SMDs) with bottom-side cooling necessitate thermal vias or dedicated heat sinks that are integrated into the circuit board. Alternatively, top-side cooling architectures can minimize thermal interface losses and mitigate the risk of thermal runaway caused by switching losses [8].

## 3. Fabrication and integration technologies of GaN power devices

The research progress of GaN materials was slow due to difficulties in acquiring suitable substrates, high dislocation densities, and the challenges in achieving p-type materials. Nevertheless, with the progress in material growth and device processing after the 1990s, these issues have been gradually resolved. This chapter provides an overview of GaN device manufacturing, focusing on two key stages: epitaxial material preparation and semiconductor-specific techniques.

### 3.1. GaN epitaxial growth and material quality control

The primary epitaxial growth methods for GaN films are metal-organic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE), and hydride vapor phase epitaxy (HVPE). Of these, MOCVD is the most widely used for high-quality growth, while HVPE is generally employed as a complementary technique to both MBE and MOCVD [9]. In particular, MOCVD is a vapor-phase epitaxy method that forms single-crystal layers by transporting gaseous compounds containing the elements of the epitaxial layer to the substrate surface for chemical reactions. Despite challenges such as potential contamination from organic metal sources and high precursor consumption, large-scale manufacturing can be achieved through real-time laser monitoring of surface conditions. MBE, on the other hand, involves the deposition of atomic or molecular beams onto a heated substrate in an ultra-high vacuum environment, where they undergo chemical reactions to form single-crystal films. It offers advantages such as lower growth temperatures, high purity, excellent uniformity, and clear interfaces. However, the ultra-high vacuum requirements result in high maintenance costs, and the slow growth rate limits its commercial scalability.

The performance and efficiency of GaN power devices heavily depend on the epitaxial growth of GaN and related alloys. Common substrates for GaN epitaxy include GaN, SiC, sapphire ($Al_2O_3$), and Si. High-quality GaN epitaxial layers with dislocation densities below $10^6$ $cm^{-2}$ can be achieved using native free-standing substrates, but their high cost and limited wafer diameter restrict the large-scale, cost-effective production of GaN power devices. SiC substrates offer high thermal conductivity and low lattice mismatch with GaN but are costly, while Si substrates are cheaper but suffer from

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significant mismatch, causing film cracking and high dislocation densities. To enhance GaN epitaxial quality, patterned substrates and buffer layer technologies are commonly employed. For example, chemically etched patterned sapphire substrates promote lateral epitaxial overgrowth, thereby effectively reducing dislocation densities and enhancing film quality by alleviating stress [10]. Heterogeneous substrates exhibit varying lattice and thermal mismatches with GaN, leading to higher dislocation densities. MOCVD combined with an AlN buffer layer enables high-quality GaN epitaxy on sapphire, addressing incompatibility in high-mismatch systems while offering nucleation centers and stress-relief mechanisms [11]. Building on this approach, the two-step growth process with low-temperature buffer layers has become the standard for high-quality GaN epitaxy.

### 3.2. GaN device fabrication and surface engineering

Substrate contamination arises from airborne particulates and elemental impurities adhering to the semiconductor surface, as well as residues from subsequent processes such as photoresist. Inorganic contaminants react with the substrate surface, while organic contaminants tend to adhere to it. Thus, the cleaning process removes organic contaminants first, then inorganic impurities [11].

Photolithography is a critical process that transfers mask patterns onto the substrate using the photosensitivity of photoresist. The standard procedure includes three main stages, beginning with substrate pretreatment, which includes cleaning, dehydration baking, spin-coating photoresist, and soft baking. This is followed by pattern transfer via mask alignment, exposure, and post-exposure baking, culminating in pattern development through chemical development and hard baking.

The device isolation process prevents crosstalk between components on the same substrate. The primary GaN isolation methods include mesa etching and ion implantation. Mesa etching offers simplicity and stability, whereas ion implantation achieves high-precision interface isolation with enhanced effectiveness [12]. Given the chemical stability of GaN, plasma dry etching is commonly employed, integrating high-energy ion sputtering with reactive gas chemical etching. However, ion bombardment can introduce deep-level defects at mesa sidewalls, forming tunneling paths that increase gate leakage [13]. For reliable pinch-off, the gate must extend over the mesa edges.

The metallization process encompasses ohmic contact formation for the source/drain and gate electrode deposition. It begins with rapid thermal annealing to promote solid-state interdiffusion in the source/drain multilayer metals, where precise temperature control is crucial for achieving low contact resistance [14]. Before metal deposition, surface passivation is implemented to suppress interface state leakage in Schottky gate structures. Finally, in AlGaN/GaN HFETs, gate dielectric optimization helps regulate barrier height, reducing off-state leakage and switching losses while overcoming the limitations of conventional designs.

The performance of experimental devices still deviates significantly from theoretical predictions, with GaN surface states identified as the primary cause of current collapse. Existing studies indicate that surface states caused by AlGaN dangling bonds, epitaxial defects, and process-induced damage result in high surface state densities, which reduce the two-dimensional electron gas concentration, induce current collapse, and increase dynamic on-resistance [15]. As such, surface passivation is crucial for device performance, and various insulating materials such as $SiO_2$ and AlN have been explored as passivation layers. Additionally, the natural formation of gallium suboxide ($GaO_x$) on GaN surfaces in ambient air exacerbates gate leakage and high-frequency current collapse: thermal treatment has been shown to effectively modify $GaO_x$ morphology, mitigating surface state effects and improving device performance [16].

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## 4. Major reliability challenges of GaN in power electronics

Reliability remains a critical concern for GaN-based HEMT devices post-deployment, significantly influencing their practical applicability. Key reliability challenges include contact degradation, hot electron effects, and inverse piezoelectric phenomena.

### 4.1. Hot carriers and trap generation

Under high drain-gate voltage stress, GaN HEMT devices may undergo irreversible degradation, primarily due to the hot electron effect. Although high gate currents often obscure this phenomenon, experimental studies have observed impact ionization. High-energy electrons gain sufficient energy under a strong electric field, potentially inducing trap generation at the AlGaN/GaN interface or the passivation layer/GaN cap interface, leading to depletion region expansion between the gate and drain. This trap effect increases drain resistance and further reduces the drain saturation current , impacting device conduction characteristics and power output capability. Also, trap accumulation can cause an increase in dynamic on-resistance, resulting in higher switching losses and reduced system efficiency. Therefore, optimizing device structure and materials to suppress trap effects is crucial for enhancing the reliability of GaN HEMTs.

### 4.2. Contact degradation

The stability of metal-semiconductor contacts directly influences the long-term reliability of GaN HEMTs. Prior studies showed that under high-temperature DC stress, both Pt/Au Schottky contacts and Ti/Al/Pt/Au ohmic contacts exhibit an increase in Schottky barrier height. This change mainly results from the consumption of the interfacial layer between the Schottky contact and the AlGaN layer, leading to a positive shift in both Schottky barrier height and pinch-off voltage, along with a reduction in drain saturation current [17]. In addition, high-temperature stress can induce alloying and metal diffusion at the metal-semiconductor interface, further increasing contact resistance. This degradation negatively affects switching characteristics and power transmission efficiency, posing challenges for high-performance applications. Research indicates that annealing unstressed devices after fabrication reduces the influence of interfacial layers between the gate and semiconductor. In comparison to non-annealed devices, annealed devices demonstrate significantly lower degradation, highlighting the critical role of interface engineering and thermal treatment in maintaining contact stability.

### 4.3. Inverse piezoelectric effects

The degradation of GaN HEMT devices under high reverse gate bias involves multiple synergistic failure mechanisms. In AlGaN/GaN heterostructures, intrinsic lattice mismatch induces interfacial tensile strain, which intensifies under high voltage and thermal stress due to inverse piezoelectric effects, eventually leading to strain relaxation. Moreover, localized breakdown of the surface oxide layer creates pit-like defects, compromising the integrity of the barrier layer. And these defects can propagate via the AlGaN barrier, further deteriorating interface quality. The high-field environment promotes the proliferation of point defects, forming numerous recombination centers that act as carrier scattering and leakage pathways. Thus, breakdown voltage decreases, leakage current rises, and overall electrical performance deteriorates [18]. To mitigate degradation induced by inverse piezoelectric effects, optimizing stress management in the AlGaN barrier and implementing high-quality passivation and interface engineering are crucial for enhancing reliability under high voltage.

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## 5. Conclusion

GaN power integration technology holds great potential due to its superior material properties but still faces challenges in fabrication and reliability. This paper traces the development of GaN power devices, examining material characteristics, fabrication processes, and key reliability concerns. The results demonstrate that device isolation is crucial for high-voltage applications, while balancing performance improvements with cost efficiency remains a key consideration. Future advancements will depend on interdisciplinary collaboration to optimize device structures, enhance manufacturing techniques, and address long-term reliability bottlenecks, thus enabling broader adoption of GaN in emerging technologies.

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