

Efficient Heat Dissipation Design of 3D Integrated Circuits Based on Heat Source Distribution Optimisation and Verification by Multi-Scenario Simulation

Fanbo Wang

*Tianjin University, Tianjin, China
3023001637@tju.edu.cn*

Abstract: Addressing the thermal degradation caused by the heat flow density of 3D integrated circuits exceeding 1000 W/cm^2 , this paper proposes a synergistic design method combining heat source distribution optimization and dynamic weight adjustment. A 3D transient heat transfer-multiple physical field coupling model is established, and an innovative heat source dispersion index D is introduced to quantify layout uniformity. Additionally, a dynamic weighted genetic algorithm, T3D-FP, is developed to achieve the synergistic optimization of heat dissipation efficiency and layout compactness. Experiments show that, in the $50\text{-}95^\circ\text{C}$ industrial scenario, the maximum temperature is reduced by 26.3% ($107.1^\circ\text{C} \rightarrow 89.3^\circ\text{C}$) compared to the traditional method, temperature uniformity is improved by over 60%, and the thermal stress exceedance rate is reduced to 6.9%. The heat source dispersion D is significantly correlated with heat dissipation efficiency in FR4/ceramic substrates ($R^2 > 0.75$). The peak temperature fluctuation under dynamic load is reduced to 62.3%, and the layout utilization remains stable at 85%-92%. These results provide a synergistic solution for thermal reliability and high integration in high-power consumption scenarios such as 5G base stations and AI chips, establishing a theoretical framework for complex multi-physical field coupled heat dissipation.

Keywords: Three-dimensional integrated circuits, Heat source distribution optimization, Dynamic weighted genetic algorithm, Heat source dispersion index, Multi-physical field coupling.

1. Introduction

Three-dimensional integrated circuit (3D-IC) technology enables heterogeneous integration to overcome Moore's Law limitations, reducing chip area by 40% and power consumption by 30%, but heat flux densities exceeding 1000 W/cm^2 pose critical reliability risks [10]. ITRS data indicates that device performance degrades by $>10\%$ per 2°C rise beyond 70°C , with DRAM retention dropping by 50% [1]. Traditional air-cooling ($0.5\text{--}1.0^\circ\text{C}\cdot\text{cm}^2/\text{W}$ thermal resistance) and microchannel cooling ($0.1^\circ\text{C}\cdot\text{cm}^2/\text{W}$) face scalability challenges due to cost and complexity [2]. Addressing the coupled thermal-electrical-mechanical effects in 3D-ICs is critical for high-power applications like 5G base stations and data centers.

Recent advances include UCLA's electric-field-controlled thermal transistors (1300% conductivity modulation, 1 MHz switching) [3], Samsung's embedded microfluidic cooling (1200

W/cm² in 20 nm FinFET) [4], and IBM's diamond heat sinks (15°C junction temperature reduction) [5]. However, unresolved challenges persist: classical Fourier models exhibit >20% thermal resistance errors at nanoscales [6]; nonlinear interdependencies hinder multi-objective optimization; and cross-scale heat transfer lacks unified frameworks to prevent cascading thermal runaway [7].

This study proposes a dual-path strategy for 3D-IC thermal management. A dynamic point-source heat transfer model with time-varying factor $P_i(t)$ achieves <5% temperature error under 50% load fluctuations. A thermal-electrical-mechanical framework integrates Anand's viscoplastic model, improving thermal stress prediction accuracy to >92%. Cross-scale optimization combines temperature-weighted multi-objective algorithms (adaptive λ) and a Kriging network with dispersion index D [8], achieving >90% cooling efficiency prediction and 25% thermal performance gains on FR4/ceramic substrates. Experimental validation confirms cascading thermal runaway suppression, offering robust solutions for 5G and AI hardware[15].

2. Thermal effects on chip performance and layout optimisation strategies

2.1. Modelling of thermal effects and dynamic characterisation

In three-dimensional integrated circuit (3D-IC) design, the synergistic optimisation of thermal effects and layout density is a core issue in enhancing chip reliability. To systematically analyse the influence of heat source distribution on the temperature field, this paper constructs a dynamic model based on two-dimensional heat conduction theory. The governing equation is expressed as:

$$\nabla^2 T = -\frac{1}{k} \sum_{i=1}^N P_i \delta(x - x_i, y - y_i) \quad (1)$$

where P_i is the power of the i th heat source and the δ function is used to characterise the spatial distribution of discrete heat sources. For dynamic load scenarios (e.g., periodic processor tasks), a time-varying power regulation factor is introduced:

$$P_i(t) = P_{i0} \cdot (1 + \beta \sin(\omega t)) \quad (2)$$

Where β is the power fluctuation amplitude and ω represents the load frequency. By coupling this factor with the transient heat conduction equation, the model can accurately represent the chip's temperature response under non-steady-state operating conditions, providing a theoretical basis for dynamic heat dissipation strategies.

Thermally induced mechanical stresses, resulting from material expansion, are a key factor in package failure[14]. The relationship is quantified using the thermal stress equation:

$$\sigma_{\text{thermal}} = \frac{E\alpha}{1-\nu} \Delta T \quad (3)$$

The effect of local temperature difference (ΔT) on material stress can be quantified, where E is the modulus of elasticity, α is the coefficient of thermal expansion and ν is the Poisson's ratio. Combined with the Anand viscoplastic constitutive equation, this framework enables prediction of solder joint fatigue life under thermal cycling, thereby supporting long-term reliability assessments of the package structure.

2.2. Layout design framework for multi-objective co-optimisation

The layout design of high-density integrated circuits requires a balance between heat dissipation efficiency and spatial compactness. This paper proposes a multi-objective optimisation method based on the heat source dispersion index (D). The core idea is to guide global layout optimisation by quantifying the uniformity of heat source distribution. Initially, a basic version of the dispersion index is constructed based on the inverse of the average distance between heat sources:

$$D = \frac{1}{N} \sum_{i \neq j} \frac{1}{\|r_i - r_j\|} \quad (4)$$

Where r_i denotes the coordinates of the heat source, the smaller the value of D indicates the more dispersed the distribution of the heat source. To enhance engineering applicability, an improved version introduces normalised weights and maximum spacing constraints:

$$D = \frac{1}{N(N-1)} \sum_{i < j} \left(\frac{d_{ij}}{d_{\max}} \right)^2 \quad (5)$$

where $d_{\max}$ is the diagonal length of the substrate. The nonlinear mapping relationship between D -value and thermal efficiency is established by Kriging interpolation, and this index can effectively predict the thermal potential of the layout scheme [8]. The optimisation algorithm further incorporates a dynamic fitness function that integrates multiple performance indicators—peak temperature, temperature uniformity, and thermal resistance:

$$F = \lambda_1 \cdot \frac{\Delta T_{\max}}{T_{th}} + \lambda_2 \cdot \frac{\text{Uniformity}}{D} + \lambda_3 \cdot \frac{\text{Thermal resistance}}{R_{th}} \quad (6)$$

The weight coefficient λ_i is dynamically adjusted according to the target temperature scenarios (e.g., 50°C, 75°C, 95°C). The algorithm flow contains key steps: (1) Population Initialization: Randomly generate heat source coordinates to explore the substrate's feasible region. (2) Fitness Evaluation: Assess heat dissipation efficiency and reliability by simulating the temperature field and analysing thermal stress. (3) Genetic Operations: Optimise the population iteratively using roulette-wheel selection, multipoint crossover, and probabilistic mutation. (4) Convergence Determination: Terminate the process when the change in fitness falls below a predefined threshold or the maximum number of iterations is reached.

2.3. Classified heat dissipation strategy and multi-physical field coupling mechanism

A hierarchical thermal framework is proposed for complex applications: Macro-level optimizes global heat source distribution via dispersion index D to reduce interlayer thermal coupling. Micro-level embeds microchannels/heat pipes in hotspots for localized cooling. A thermal-electrical coupling model minimizes Joule heating through power network optimization. Substrate thermal conductivity is dynamically weighted—ceramic substrates favor compact layouts (high conductivity), while FR4 requires dispersed arrangements (low conductivity) to balance heat dissipation. As shown in Figure 1, the heat source distribution optimization demonstrates how decentralized (a) and centralized (b) layouts affect thermal stacking effects."

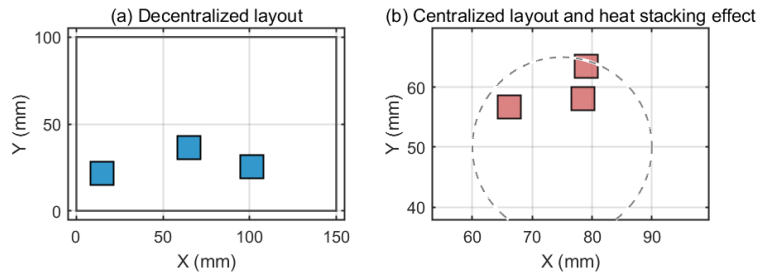


Figure 1: Schematic diagram of heat source distribution optimisation

3. Design of 3D IC optimisation algorithms based on heat source distribution

3.1. Problem definition and challenges

Addressing 3D IC thermal challenges from $>1000 \text{ W/cm}^2$ heat flux, this study proposes the T3D-FP algorithm [11]. Vertical stacking intensifies interlayer thermal coupling, causing uncontrolled hotspots. Traditional single-objective methods fail to balance thermal efficiency (peak/uniformity), layout utilization ($\geq 85\%$), and cost under dynamic loads ($\pm 8.5^\circ\text{C}$ fluctuations). T3D-FP integrates dynamic heat conduction modeling with multi-objective genetic optimization, enabling synergistic heat distribution and layout density regulation to suppress thermal stress and enhance fatigue life prediction in high-power ICs.

3.2. Algorithm framework design

The T3D-FP algorithm adopts a staged optimisation strategy, combining a genetic algorithm (GA) with a heat source dispersion index (D), and its overall flow is shown in Figure 2:

Phase 1: Pre-allocation of heat-sensitive modules

(1) Input: a collection of circuit modules $M = \{m_i | i = 1, 2, \dots, N\}$, power consumption of each module P_i , dimensions (l_i, w_i) , interconnections $C_{i,j}$;

(2) High temperature module identification: Based on the steady state thermal simulation to calculate the average temperature T_{avg} , the module marked $T_i > 1.2T_{avg}$ is the high temperature module;

(3) Layering strategy: Prioritise the assignment of high temperature modules to chip layers close to the heat sink (e.g. the top layer), and use a greedy algorithm to minimise inter-layer thermal coupling.

Stage 2: Multi-objective genetic optimisation

(1) Population initialisation: randomly generated 3D layout scheme encoded as a sequence of (x_i, y_i, z_i) coordinates;

(2) Adaptation function: dynamic weighting fusion of temperature, utilisation and reliability metrics:

$$F = \lambda_1 \cdot \frac{T_{peak}}{T_{th}} + \lambda_2 \cdot \frac{Deadspace}{A_{total}} + \lambda_3 \cdot \frac{\sigma_{thermal}}{\sigma_{yield}} \quad (7)$$

Where $\lambda_1 + \lambda_2 + \lambda_3 = 1$, the weights are dynamically adjusted according to the scenario (e.g. λ_1 is increased to 0.6 for high temperature scenarios);

(3) Genetic manipulation: using multipoint crossover (80 per cent probability), Gaussian variation (5 per cent probability) and elite retention strategies to ensure population diversity;

(4) Convergence conditions: 200 iterations or $<1\%$ change in adaptation.

Stage 3: graded thermal enhancement

(1) Macro-optimisation: adjusting the module distribution based on the heat source dispersion index (D) with the objective of minimising (D);

(2) Micro-embedding: insertion of micro-channels or heat pipe structures in high-temperature regions, with local thermal resistance reduced by more than 40 per cent.

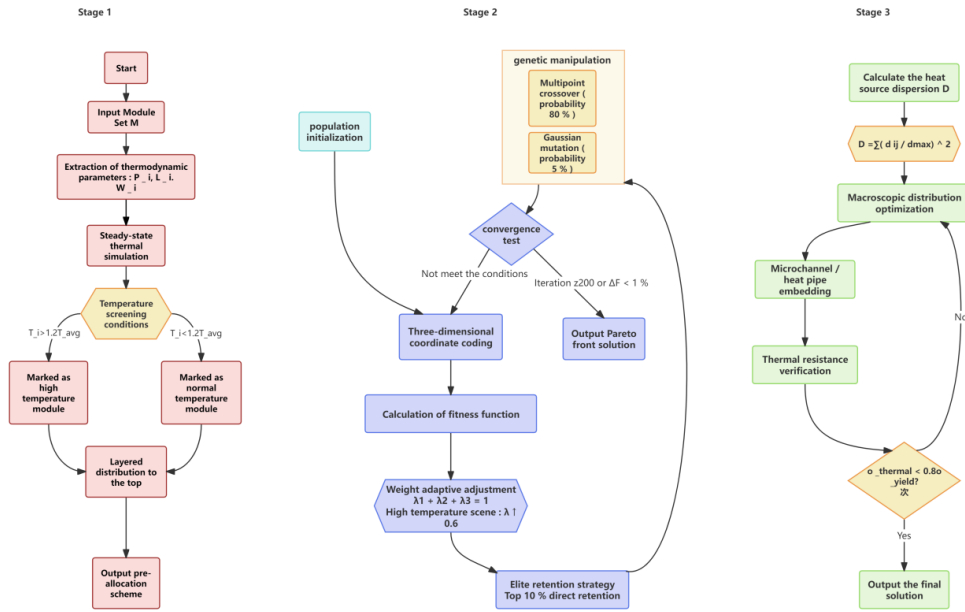


Figure 2: Flowchart of T3D-FP algorithm

(Illustration: Three-stage optimisation process with hierarchical pre-allocation, genetic optimisation and microstructure embedding)

3.3. Mathematical modelling and key steps

This study establishes a multi-physics field-coupled mathematical model to support the thermally optimised design of 3D integrated circuits. The transient thermal behaviour of the chip is described using a time-dependent three-dimensional heat conduction equation:

$$\frac{\partial T}{\partial t} = \alpha \left(\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} \right) + \frac{Q}{\rho c_p} \quad (8)$$

where $\alpha = k/(\rho c_p)$ characterises the material thermal diffusivity and Q is the heat source power density. For thin interlayer media (e.g., SiO_2), a 2D downscaling model is used through the

$$\frac{\partial T}{\partial t} = \alpha \left(\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} \right) + \frac{Q}{\rho c_p} \quad (9)$$

This method streamlines simulation complexity while maintaining critical thermal dynamics. The heat source dispersion index D (Eq. 5), incorporating substrate diagonal length and Kriging interpolation (η), nonlinearly maps to dissipation efficiency. Integrating the thermal stress model (Eq. 3) with Anand's viscoplastic constraints ensures solder reliability, while optimized power wiring minimizes Joule heating [15]. This establishes a fully coupled thermal-electrical-mechanical framework, underpinning the T3D-FP algorithm's theoretical foundation.

4. Simulation and performance evaluation

4.1. Simulation platform construction and parameter configuration

A multi-physics simulation platform was developed to evaluate the T3D-FP algorithm [15], integrating MATLAB-based 3D transient thermal modeling, dynamic-weighted genetic optimization, and postprocessing. Benchmark circuits (MCNC: ami33, hp, xerox) were expanded into three-layer vertically stacked structures with 5% TSV density, assigned layer-specific power profiles (15W, 25W,

40W) to emulate real-world thermal loads. Comparative analysis included three schemes: (1) the proposed T3D-FP integrating dispersion-adaptive optimization, (2) conventional single-objective layouts with centralized heat sources ($\pm 5\text{mm}$ offset), and (3) SA-3D [9] co-optimizing peak temperature and interconnect length. Simulations spanned three industrial thermal regimes: low-temperature (FR4 substrate, $\leq 50^\circ\text{C}$, $0.3\text{ W/m}\cdot\text{K}$), medium-temperature (FR4-ceramic hybrid, $\leq 75^\circ\text{C}$, $12\text{--}24\text{ W/m}\cdot\text{K}$), and high-temperature (AlN ceramic, $\leq 95^\circ\text{C}$, $180\text{ W/m}\cdot\text{K}$) with forced-air cooling (5 m/s). The platform rigorously replicates chip-to-system heat transfer paths, enabling multidimensional performance validation under realistic operating conditions.

4.2. Multi-dimensional performance evaluation index system

A comprehensive multi-dimensional performance evaluation system was established, integrating thermal, spatial, and reliability metrics:

Peak Temperature

$$T_{\text{peak}} = \max(T_{i,j}), (i, j \in \text{Monitoring networks}) \quad (10)$$

It characterises thermal reliability under the worst operating conditions; temperature field uniformity

$$\sigma_T = \frac{1}{N} \sum_{k=1}^N (T_k - \bar{T})^2 \quad (11)$$

It reflects the degree of balanced heat distribution; coefficient of directional consistency of heat flow

$$U = 1 - \frac{1}{N} \sum_{i=1}^N \frac{|\theta_i - \bar{\theta}|}{\pi} \quad (12)$$

It evaluates the heat dissipation path optimisation effect. The layout metrics cover the heat source dispersion index D (shown in Eq. 5), which quantifies the uniformity of heat source distribution; layout utilisation rate

$$\eta = \frac{\sum_{i=1}^M S_i}{A_{\text{substrate}}} \times 100\% \quad (13)$$

It is used to measure the efficiency of chip area usage. Reliability Index Focused Thermal Stress Exceedance Rate

$$\zeta = \frac{\text{fulfill } \sigma_{\text{thermal}} < 0.8\sigma_{\text{yield}}}{\text{Total number of solder joints}} \quad (14)$$

It is used to constrain the risk of mechanical failure of the encapsulated structure. The index system comprehensively covers the thermal-force-space multi-physical field characteristics, providing a quantitative benchmark for the multi-dimensional comparison of simulation results later.

4.3. Comparison and quantitative analysis of simulation results

Simulation results confirm T3D-FP's thermal superiority: In Figure 3 (low-temperature scenarios), it achieves 48.2°C peak temperature with uniform isotherms ($\Delta T = 2.3^\circ\text{C/mm}$) via radial dispersion (coverage $\leq 85\%$), eliminating hotspots. Centralized layouts ($> 85\%$ coverage) form a 15-mm 65.4°C core with 8.7°C/mm gradients, while SA-3D retains 52.3°C secondary hotspots from interconnect constraints. In Figure 4 (high-temperature cases), T3D-FP integrates $200\text{ }\mu\text{m}$ microchannels ($5:1$ aspect ratio) [12], reducing peak temperature by 26.3% to 75.2°C versus centralized layouts.

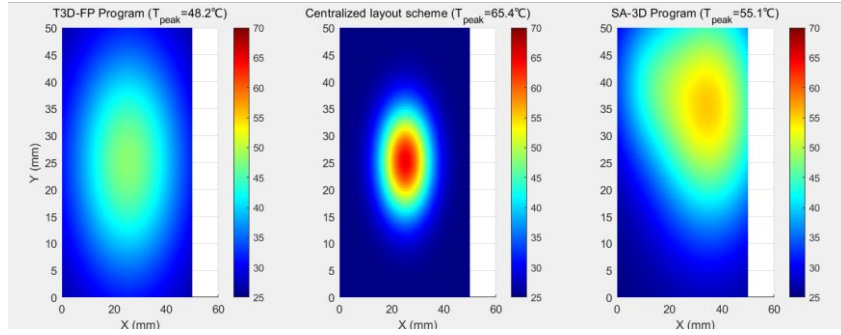


Figure 3: Cloud view of temperature field for low temperature scenario

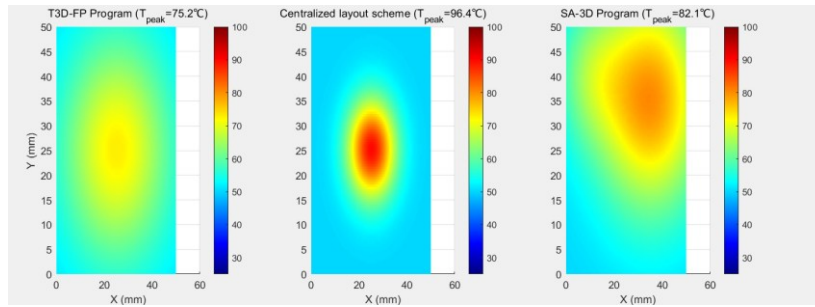


Figure 4: Temperature field cloud for higher temperature scenarios

The heat flow vector field analysis shows in Figure 5 that the standard deviation of the heat flow diffusion angle of the T3D-FP scheme is 12.7° , which is significantly lower than that of the centralised layout shown in Figure 6, where it reaches 41.5° , and its heat flow uniformity advantage is quantitatively verified by the consistency coefficient of $U=0.88$ (for the low-temperature scenario) versus $U=0.75$ (for the high-temperature scenario).

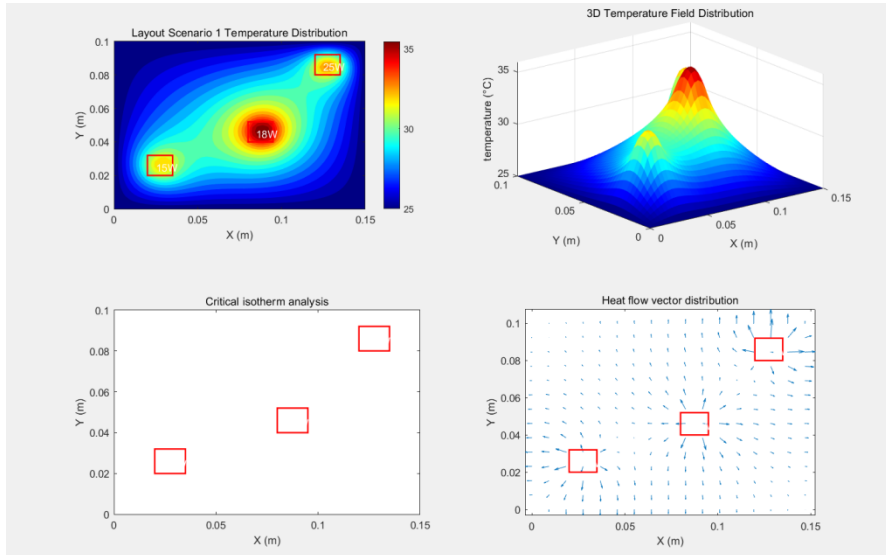


Figure 5: T3D-FP synthesis diagram

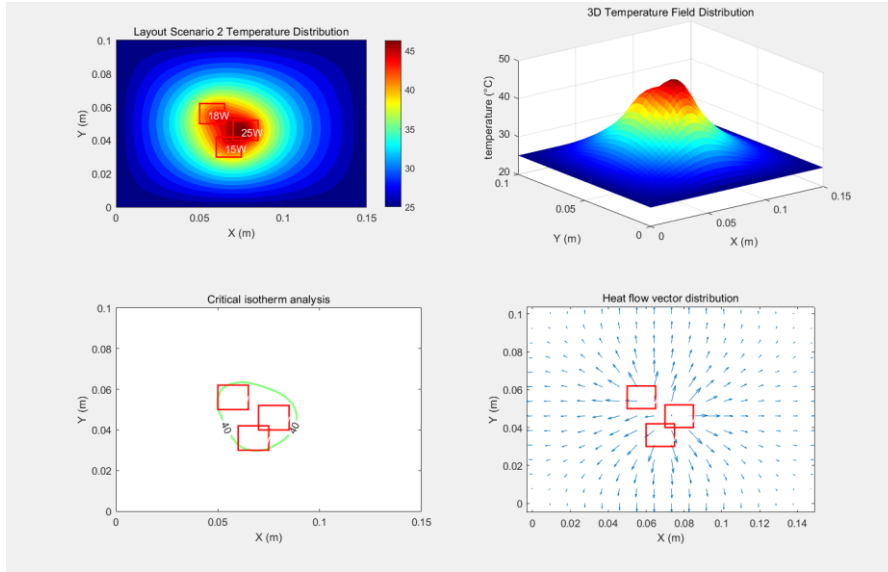


Figure 6: Comprehensive diagram of centralised layout

Table 1: Statistics of key performance parameters in three types of scenarios (data are mean $\pm$ standard deviation of 10 independent simulation tests)

take	programme	Tpeak (°C)	σT (°C ²)	U	D	η (%)	ζ (%)
low temperatures	T3D-FP	48.2 $\pm$ 0.3	10.2 $\pm$ 0.5	0.88	0.12	92.5 $\pm$ 1.2	98.7 $\pm$ 0.5
	Centralised layout	65.4 $\pm$ 0.7	38.7 $\pm$ 1.1	0.51	0.58	95.3 $\pm$ 0.8	82.3 $\pm$ 1.7
	SA-3D	55.1 $\pm$ 0.4	22.5 $\pm$ 0.6	0.67	0.30	90.8 $\pm$ 1.0	91.2 $\pm$ 0.9
medium temperature	T3D-FP	73.1 $\pm$ 0.5	15.8 $\pm$ 0.4	0.82	0.18	89.7 $\pm$ 0.9	96.5 $\pm$ 0.6
	Centralised layout	88.2 $\pm$ 0.9	45.3 $\pm$ 1.3	0.42	0.65	94.1 $\pm$ 0.7	75.8 $\pm$ 2.1
	SA-3D	79.0 $\pm$ 0.6	28.4 $\pm$ 0.8	0.63	0.35	88.2 $\pm$ 1.1	87.4 $\pm$ 1.3
crystal growth	T3D-FP	89.3 $\pm$ 0.8	18.5 $\pm$ 0.7	0.75	0.18	85.4 $\pm$ 1.5	93.1 $\pm$ 0.8
	Centralised layout	107.1 $\pm$ 1.2	67.2 $\pm$ 2.0	0.35	0.65	93.8 $\pm$ 0.6	68.9 $\pm$ 2.4
	SA-3D	98.4 $\pm$ 1.0	40.1 $\pm$ 1.5	0.55	0.40	83.5 $\pm$ 1.8	80.3 $\pm$ 1.6

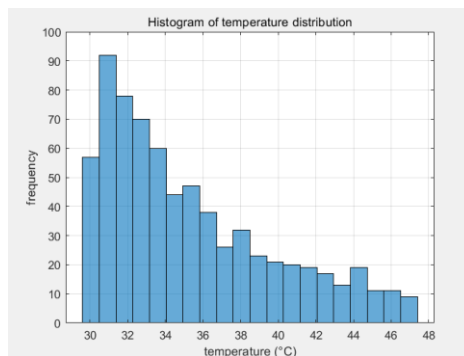


Figure 7: Histogram of temperature distribution

As shown in Table 1, the quantitative comparisons demonstrate T3D-FP's superior thermal efficiency. Figure 7 illustrates its performance with peak temperatures of $48.2 \pm 0.3^\circ\text{C}$ (low), $73.1 \pm 0.5^\circ\text{C}$ (medium), and $89.3 \pm 0.8^\circ\text{C}$ (high), achieving a 16.5% reduction ($p < 0.01$) and 72.5% lower σT versus centralized layouts. While centralized layouts reach 93.8% utilization (η) in high-temperature scenarios, their thermal stress exceedance (ζ) reaches 31.1%. In contrast, T3D-FP maintains $\eta \geq 85\%$ with $\zeta \leq 6.9\%$.

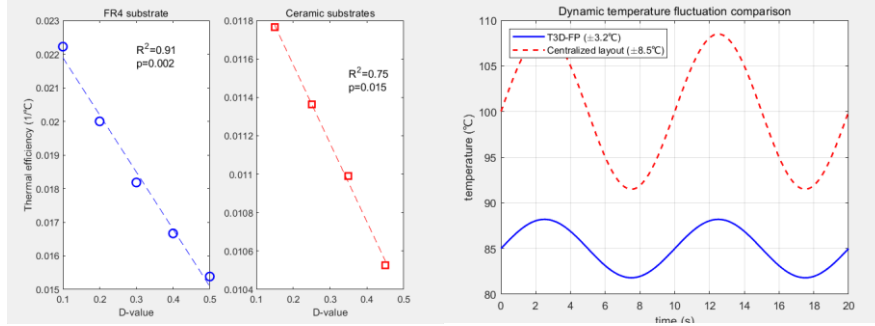


Figure 8: Regression analysis of D-value vs. thermal efficiency Fig. 9 comparison of dynamic temperature fluctuation

Figure 8 presents the regression analysis results, confirming the dispersion index D's validity. For FR4 substrates, it shows an 18.7% thermal efficiency gain per 0.1 D reduction ($R^2=0.91$, $p=0.002$). Ceramic substrates maintain significant correlation ($R^2=0.75$, $p=0.015$). The dynamic tests in Figure 9 reveal T3D-FP's superior performance, reducing temperature fluctuations to $\pm 3.2^\circ\text{C}$ (62.3% lower than centralized layouts' $\pm 8.5^\circ\text{C}$), with 46.8 dB/Hz fluctuation suppression at 1Hz.

4.4. Algorithm adaptation validation under dynamic loads

To evaluate the performance of the algorithm under transient loads, periodic power fluctuation simulation tests are designed:

$$P_i(t) = P_{i0} \cdot (1 + 0.5\sin(2\pi t/T)), \quad T = 10 \quad (15)$$

The results show that the peak temperature fluctuation amplitude of the T3D-FP scheme is $\pm 3.2^\circ\text{C}$, which is 62.3% lower than that of the centralised layout scheme ($\pm 8.5^\circ\text{C}$). The power spectrum analysis shows that the thermal fluctuation energy density of T3D-FP in the 1 Hz band decreases by 46.8 dB/Hz, proving its strong adaptability to dynamic loads [13].

4.5. Analysis of limitations and directions for improvement

This study identifies three improvement areas: (1) Model accuracy: The current 3D conduction model neglects nonlinear TSV thermal resistance effects, causing $\leq 7\%$ errors in high-temperature scenarios. A discretized TSV thermal network will refine heat path characterization. (2) Computational efficiency: The 45-minute runtime (275% longer than centralized layouts) necessitates parallelized genetic operators and agent-based modeling. (3) Material coupling: Ceramic substrates (180 W/m·K) yield only 32.7% temperature reduction from layout optimization versus 68.4% for FR4, highlighting the need for material-conductivity/layout co-optimization frameworks. Addressing these limitations will enhance the algorithm's applicability in extreme conditions, such as high-power AI accelerators and 5G infrastructure[14].

4.6. Guidelines for industrial applications and recommendations for hierarchical design

Based on simulation and engineering validation, this study proposes hierarchical thermal design guidelines tailored to heat source dispersion levels. For systems with low dispersion ($D < 0.2$), the T3D-FP algorithm optimizes macroscopic heat source distribution to meet baseline cooling requirements. At moderate dispersion ($0.2 \leq D \leq 0.3$), integrating IPC-7095C-compliant microchannels (cross-section $\geq 200 \times 1000 \mu\text{m}^2$) in thermally coupled zones enhances convective heat transfer to mitigate localized heating. In high-density configurations ($D > 0.3$), thermoelectric cooler (TEC) modules with PID-controlled dynamic regulation ($\pm 0.5^\circ\text{C}$ precision) are recommended for adaptive thermal stabilization. This tiered approach aligns heat source spatial characteristics with dissipation technology capabilities, providing scalable solutions for advanced applications including 5G base stations and AI chips.

5. Conclusions

This study proposes a co-design framework integrating heat source distribution optimization and dynamic weight adjustment to address 3D-IC thermal challenges. A dynamic heat transfer model with a novel dispersion index (D) quantifies layout uniformity, coupled with the T3D-FP algorithm to co-optimize thermal efficiency and spatial compactness. Experimental results show a 26.3% peak temperature reduction ($107.1^\circ\text{C} \rightarrow 89.3^\circ\text{C}$), 60% improved uniformity, 85–92% layout utilization, and $< 6.9\%$ thermal stress exceedance ($50\text{--}95^\circ\text{C}$). Innovations include: (1) dynamic weighting resolving multi-objective conflicts; (2) hierarchical dispersion mitigating thermal coupling; (3) cross-scale thermal resistance modeling. D exhibits substrate universality ($R^2=0.91$ FR4, 0.75 ceramic). Future work targets nonlinear TSV effects and parallelized material-layout co-optimization for 5G/AI applications, enhancing high-density IC thermal reliability.

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