

Research on the Reliability of Semiconductor Chips under Extreme Conditions and Strategies

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Abstract. Semiconductor chips face multiple challenges such as high temperatures, radiation, and mechanical vibrations in extreme environment applications like aerospace, automotive electronics, and nuclear energy. Their performance stability is crucial for system reliability. This research systematically analyzes the failure modes of chips under the combined action of multiple fields including temperature, radiation, and humidity. By adopting a technical approach that integrates in-situ testing, numerical simulation, and failure analysis, it reveals the primary failure mechanisms, such as gate oxide layer breakdown and metal interconnect electromigration. The novel multi-layer passivation structure and low-stress packaging process offer superior protection against chip failures in extreme environments compared to traditional methods. Future research should focus on in-depth studies of high-k gate dielectric material modifications to improve their radiation tolerance and enhance the overall reliability of chips in radiation-intensive environments.

Keywords: Semiconductor chips, Extreme conditions, Reliability, Failure analysis, Packaging technology, Radiation effects

1. Introduction

With the rapid development of technology, semiconductor chips are being used more and more widely in extreme environments, such as in Mars rovers and nuclear reactor monitoring. However, existing chips have performance bottlenecks in high-temperature, radiation, and other environments. Although previous studies have explored some failure phenomena, the failure mechanisms of chips under the combined action of multiple physical fields and strategies for improving reliability still need to be further studied [1-3]. Against this background, this paper focuses on the reliability of semiconductor chips under extreme conditions, with a particular emphasis on researching the corrosion failure mechanism of chips in a combined high-temperature and high-humidity environment, the law of the impact of ionizing radiation on the threshold voltage of CMOS devices, the fatigue failure process of solder joints caused by mechanical vibration, and the corresponding strategies for improving reliability. This study contributes to provide theoretical support for the design of chips dedicated to extreme environments and promote the development of related fields.

2. Analysis of failure mechanisms under extreme conditions

2.1. Influence of thermal effects

The junction temperature significantly affects carrier mobility. During chip operation, the heat generated internally elevates the junction temperature. As the junction temperature rises, the lattice vibration intensifies, and the scattering probability between carriers and the lattice increases, resulting in a decrease in carrier mobility. This affects the electrical performance of the chip. For example, the on-resistance of transistors increases, which in turn affects the performance and power consumption of the entire circuit [4].

During the thermal cycling process, due to the mismatch in the thermal expansion coefficients of the chip and the substrate, stress is generated at the interface. After multiple thermal cycles, this stress accumulates continuously, which may lead to cracks in the connection between the chip and the substrate, affecting the heat dissipation effect and the stability of the electrical connection of the chip. In severe cases, it can even cause the chip to fail [5].

2.2. Radiation damage mechanisms

The total ionizing dose (TID) effect can cause the threshold shift of MOSFETs. In a radiation environment, the atoms in semiconductor materials absorb radiation energy and undergo ionization, generating electron-hole pairs in the gate oxide layer. Some electrons and holes become trapped at trap sites, thereby altering the charge distribution within the oxide layer and causing a shift in the threshold voltage of MOSFETs, which disrupts the normal operation of the devices [6].

The soft error rate (SEE) caused by the single event effect is also an important issue. When high-energy particles strike a chip, a large number of electron-hole pairs are generated in a local area, forming a transient current. If these transient currents interfere with the internal logic state of the chip, soft errors will occur, such as data flipping in memory cells, affecting the reliability of the system [7].

2.3. Chemical corrosion effects

The penetration of chloride ions can cause the corrosion of metal layers. In a high-temperature and high-humidity environment, moisture containing chloride ions may penetrate the metal layer of the chip. Chloride ions are highly corrosive and can react chemically with metals, destroying the structure of the metal layer and forming corrosion paths, leading to a decrease in the conductivity of the metal layer or even an open circuit [8].

The water absorption of packaging materials also affects the internal circuit. After the packaging materials absorb water, the water vaporizes and expands in a high-temperature environment, which may cause the packaging to crack. At the same time, the water vapor may react chemically with the internal circuit, corroding the circuit components and affecting the electrical performance and reliability of the chip [9].

3. Testing technologies and research methods

3.1. In-situ testing platform

A temperature-controlled humidity-heat test chamber with high and low temperature adjustment functions was designed. This test chamber can simulate the high-temperature and high-humidity

conditions in extreme environments. By precisely controlling the temperature and humidity inside the test chamber, accelerated aging tests can be carried out on chips to observe the performance changes of chips in harsh environments [10].

A real-time electrical parameter monitoring system was equipped. During the test process, this system can monitor the electrical parameters of the chip in real-time, such as current, voltage, and resistance. Through the real-time monitoring of these parameters, subtle changes in chip performance can be promptly detected, thereby providing data support for analyzing the failure progression of the chip [10].

3.2. Failure analysis technologies

A scanning electron microscope (SEM) was used to observe the surface morphology of failed chips. SEM can provide high-resolution images, clearly showing the microscopic structure of the chip surface, such as the corrosion of the metal layer and the cracks at the interface between the chip and the substrate, helping to analyze the causes and locations of failures [8].

A transmission electron microscope (TEM) was used for in-depth analysis of the internal structure of the chip. TEM can observe the atomic arrangement and crystal structure inside the chip, which is of great significance for studying the breakdown mechanism of the gate oxide layer and the defects of semiconductor materials. Through TEM analysis, detailed information about the changes in the microscopic structure of the chip can be obtained, providing a microscopic basis for understanding the failure mechanism [6].

3.3. Comparative experimental research

Different types of semiconductor chips were selected for comparative testing under the same extreme environment conditions. For example, chips with different process technologies and packaging materials were used. These chips were simultaneously placed in a temperature-controlled humidity-heat test chamber. They underwent high-temperature and high-humidity aging tests. Alternatively, they were irradiated under the same radiation source [10].

By comparing the performance changes and failure times of different chips in the same environment, the influence of chip characteristics on their reliability in extreme environments was analyzed. Through such comparative experiments, the influence degree of different factors on chip reliability can be more intuitively understood, providing a reference for targeted improvement of chip reliability [1-3].

4. Typical chip failure cases

4.1. Failure analysis of power semiconductor modules

Taking the insulated-gate bipolar transistor (IGBT) as an example, a thermal runaway process occurs under short-circuit impact. When a short circuit occurs, a large current quickly passes through the IGBT, causing the chip to generate a large amount of heat. Since the heat cannot be dissipated in time, the chip temperature rises sharply, which in turn leads to more current leakage, forming a vicious cycle and ultimately resulting in thermal runaway and the failure of the IGBT [4].

The heat dissipation design has an important impact on the junction temperature distribution. An unreasonable heat dissipation design will cause the local temperature of the chip to be too high, accelerating the aging and failure of the chip. Through thermal resistance network modeling and experimental tests, it was found that optimizing the heat dissipation structure can effectively reduce

the junction temperature of the chip. For example, increasing the number and area of heat dissipation fins can achieve this. This optimization improves the reliability of the power semiconductor module [5].

4.2. Radiation response characteristics of microprocessors

Microprocessors with different process nodes have different LET (linear energy transfer) thresholds in a radiation environment. The LET threshold is an important indicator for measuring the radiation resistance of microprocessors. As the process node continues to shrink, the sensitivity of microprocessors to radiation increases, and the LET threshold decreases. This means that in the same radiation environment, microprocessors with advanced process nodes are more vulnerable to radiation damage [7].

It was found that the radiation resistance performance of microprocessors can be optimized by using a triple structure. The triple structure increases redundant circuits. When one part is damaged by radiation, other parts can continue to operate normally, thereby improving the reliability of microprocessors in a radiation environment. Through experiments and simulations, it was verified that the triple structure can effectively reduce the soft error rate and improve the radiation resistance of microprocessors [7].

5. Strategies for improving reliability

5.1. Material and structure optimization

Research was conducted on the radiation tolerance of high-k gate dielectric materials. High-k gate dielectric materials can improve the performance of chips, but in a radiation environment, their performance may decline. Through material modification, such as the addition of specific elements or the employment of specialized preparation processes, the radiation tolerance of the materials can be enhanced. This mitigation reduces the damage to the gate oxide layer induced by radiation, thereby augmenting the reliability of the chip [6].

The nano-silver sintering process has unique advantages in high-temperature packaging. The nano-silver sintering process can achieve a reliable connection between the chip and the substrate at a relatively low temperature, and has good electrical and thermal conductivity. Compared with traditional welding processes, the nano-silver sintering process can effectively reduce thermal stress and improve the stability and reliability of chips in high-temperature environments [5].

5.2. Circuit-level protection design

An anti-radiation design using redundant logic circuits was adopted. Redundant logic was set in key circuit parts. In the event of a malfunction in the primary logic circuit due to radiation interference, the redundant logic circuit can assume the workload promptly, thereby ensuring the continued operation of the circuit. By reasonably designing the layout and switching mechanism of the redundant logic circuit, the anti-radiation ability of the circuit can be significantly improved without increasing the chip area and power consumption too much [7].

The layout of the transient voltage suppressor (TVS) was optimized. TVS is used to protect chips from transient overvoltage damage. Optimizing the layout of TVS can enable it to respond to overvoltage in the shortest time and limit the overvoltage within a safe range. Through simulation and experimental analysis, the optimal layout position of TVS in the chip was determined, which

can effectively improve the protection ability of the chip against transient overvoltage and enhance the reliability of the chip [10].

6. Conclusion

In this study, a chip life prediction model under multiple stress conditions was successfully established. This model comprehensively considers the impact of multiple factors such as thermal effects, radiation effects, and chemical corrosion on the chip life, providing a powerful tool for evaluating the reliability of chips in extreme environments. At the same time, an anti-radiation ASIC design process with independent intellectual property rights was developed, improving China's independent innovation ability in the field of anti-radiation chip design. However, this study also has certain limitations. Currently, there is a lack of experimental data on the comprehensive effects of the space environment, and there is insufficient exploration of the application of new two-dimensional semiconductor materials in extreme environments. In the future, relevant experimental research can be further carried out, and intelligent health monitoring systems can be explored by integrating requirements to better meet the higher requirements for the reliability of semiconductor chips in extreme environments and promote the development of semiconductor chips in the field of extreme environment applications.

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