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Superjunction Silicon-Based Devices vs. Vertical GaN Devices: Multi-Physics Co-Optimization Strategies for New Energy Vehicle Inverters

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Abstract. New energy vehicle inverter, as the "heart" of the electric drive system power conversion unit, has its material technology directly impacting the efficiency and power density of the entire system. Currently, silicon-based super junction (SJ-Si) devices have occupied the medium-voltage market. Wide-band semiconductors such as silicon carbide (SiC) and gallium nitride (GaN), despite their high-frequency and high-voltage performance advantages, face delayed industrialization due to material defects and cost issues. This paper analyzes SJ-Si and vertical GaN power devices using multi-physics co-optimization to assess their potential for high-performance, cost-effective inverters in new energy vehicles. It employs multi-scale simulations and machine learning to compare their electric field management, electro-thermal characteristics, and fabrication costs, and reviews the latest literature on high-voltage power devices. The findings show that SJ-Si is suitable for cost-sensitive medium-voltage applications, while vertical GaN is more suitable for high-frequency and high-power density applications. The two can complement each other's performance through partition collaboration and intelligent design tools, providing new ideas for the evolution of next-generation inverter technology.

Keywords: Silicon Superjunction, Vertical GaN, Multi-physics Co-design, Electro-thermal Coupling, New Energy Vehicle Inverter

1. Introduction

New energy vehicle (NEV) inverters, as the core power conversion unit of the electric drive system, are responsible for efficiently converting direct current (DC) from the battery to alternating current (AC) for the motor, controlling motor torque and speed, and providing high-frequency excitation voltage for charging coils [1]. These inverters primarily use silicon (Si)-based devices, super junction (SJ) MOSFETs, silicon carbide (SiC) MOSFETs, and gallium nitride (GaN) HEMTs. Si-based/SJ MOSFETs dominate the 400V medium-voltage (MV) market due to their mature process, low cost, and simple driving, making them suitable for medium-power scenarios [2]. SJ structures offer lower on-resistance than traditional Si devices, fitting 600-900V MV inverters [3,4]. However, Si's physical limits restrict high-frequency/high-voltage performance. SiC MOSFETs provide high

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temperature stability, high breakdown voltage, and low on-state loss, suitable for >1.2kV systems, but face high costs and complex processes [2,5]. GaN devices feature high critical fields, ultra-fast switching speeds (MHz class), and low on-state resistance, ideal for high-frequency inverters [1,6,7]. Despite these advantages, GaN faces challenges such as high substrate costs, low thermal conductivity of sapphire substrates, and difficulties in deep trench etching and p-type doping [6,8].

Against the above background, this paper aims to systematically review the key semiconductor materials used in NEV inverters and analyze their performance, cost, and reliability. The study focuses on the behavioural changes of these materials under different operating conditions, and explores the synergistic and complementary technological paths among multiple materials by combining multi-scale simulation technology, machine learning (ML) assisted optimization, superjunction (SJ) structural innovation, and the latest breakthroughs in vertical GaN devices. This paper offers valuable insights for the development of next-generation inverters.

2. Material physical limits and breakthroughs

Studies have shown that silicon-based superjunctions (SJ-Si) have five major advantages [3,4]. One, superjunctions optimise the electric field distribution in two or even three dimensions by introducing periodically alternating N and P regions (i.e., PN column structure) within the voltage sustaining layer to form vertical or horizontal SJ-Si, the former achieving high voltage withstand and low on-resistance through longitudinal charge balancing, and the latter being compatible with the integrated circuit process, which is easy to integrate and suppresses substrate interference. Secondly, silicon superjunction devices achieve $Ron \propto VB^{1.03}$, a quasi-linear relationship, compared to the conventional silicon-based power devices with $Ron \propto VB^{2.5}$, the 600V-level Ronsp drops from 89.4mΩ·cm² to 6.54mΩ·cm², a performance improvement of more than 10 times; 600V-level FOM rises from 1.0 GW/cm² to 8.5 GW/cm², a performance improvement of 7.5 times. Third, the high-frequency dynamic characteristics of silicon-based superjunction devices are better than those of ordinary silicon-based devices. Thanks to the optimisation of the junction capacitance brought about by the charge-balanced structure (Coss/Ciss reduced by 20-30%), the unipolar conductive properties (no minority carrier storage) and the electric field homogenisation effect (improved di/dt tolerance), the switching losses are reduced by 30%-50%, and the efficiency of the work is improved by 2-3 times. Fourth, the silicon-based superjunction device in the field of high-voltage above 600V at the same time with a mature process and very low cost, while providing close to the GaN Ron, sp performance, is currently a cost-effective high-voltage power solutions. Fifth, the SJ charge balance model can be migrated to GaN polarised superjunctions, which is a bridge from silicon-based to wide-bandgap and enables partitioned collaboration between SJ-Si and GaN in inverters [5,9].

And there are three major problems with the current electric field at the vertical GaN interface. First, the electric field distortion caused by heterojunction polarisation.The spontaneous polarisation and piezoelectric polarisation effects in AlGaN/GaN heterojunctions generate high-density two-dimensional electron gas (DEG) at the interface, leading to changes in the vertical depletion region at the bottom of the Fin and enhancement of the electric field under the gate, which results in an uneven distribution of the electric field. The electric field distortion may lead to local hot spots and premature breakdown, affecting the long-term stability and switching characteristics of the device. Secondly, the amplification effect of material defects on electric field is analysed. The common defects in GaN materials mainly include: dislocation defects, point defects, interface states, impurity contamination, which affect the electric field distribution and reliability of the device. The material defects as charge traps will lead to local charge accumulation, which triggers a 3-5 times electric field amplification effect under reverse bias, which is manifested by the formation of energy band

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bending and local high electric field region at the defect interface. Thirdly, the limitation of edge termination design. These are: electric field concentration effect, i.e., edge termination still exists under high voltage, and the edge electric field can be up to 2-3 times of the body area, leading to an increase in the risk of breakdown by 30-40%, but it is difficult to achieve the ideal distribution of the electric field in the traditional structure; process sensitivity, the performance of the termination is extremely sensitive to the fluctuation of the process: a deviation of the etching angle by 5° leads to a 15% drop in the breakdown voltage, and a fluctuation of the injected dose by ±10% leads to a 50% change in the leakage current; reliability bottleneck; the reliability bottleneck. Reliability bottleneck, the edge temperature rise is 20-30°C higher than the central area, the terminal structure is the first to fail in the thermal cycle test, and the dynamic test shows that the edge degradation rate is 3 times higher than the body area; Area efficiency dilemma, the traditional terminal occupies 30-40% of the chip area, and the width of the chip needs to be increased by 8-10 μm for every 100V of withstand voltage, and the new PSJ structure improves the electric field distribution but increases the complexity of the process by 3 times [10]. The new PSJ structure improves the electric field distribution, but increases the process complexity by 3 times [11].

3. Multi-physical field synergistic optimisation mechanism

3.1. Electro-thermal coupling design

The power module of SJ-Si devices improves system reliability by introducing a copper substrate that is highly compatible with the coefficient of thermal expansion (CTE) of the silicon chip. The core technical principle is as follows:

The CTE of copper substrate is very similar to that of silicon material, and this CTE synergy design can effectively reduce the mechanical stress during thermal cycling. When the device experiences temperature fluctuations during power cycling, the difference in CTE between conventional materials (e.g. aluminium substrates) and silicon chips can lead to micro-cracks at the interface, whereas the CTE match of copper substrates can reduce thermal stresses by more than 40%. Experimental data shows that: after the integration with copper substrate, the junction temperature fluctuation range is narrowed from ±35°C to ±20°C, and this optimisation directly suppresses the thermal fatigue failure mechanism. Moreover, the reduced temperature fluctuation amplitude delays solder layer fatigue and lead bonding degradation, enabling the device to maintain a stable electrical connection under severe operating conditions, and the power cycle life is directly increased to four times that of the original design [12].

Through structural innovation, the new vertical GaN achieves a breakthrough in thermal management performance by 3D printing a pin-fin heat sink. The technology combines microneedle arrays and topology-optimised runner design to reduce the system thermal resistance to 0.15 K/W (60% lower than the traditional heat dissipation solution). This breakthrough directly meets the core demand for efficient heat dissipation in wide-band semiconductors, as the high power density applications of GaN devices, despite their low output capacitance (5 nC-Ω) and high-speed switching characteristics (150 V/ns), are still constrained by the heat build-up. The new heat sink increases the effective heat dissipation surface area through a 3D microneedle structure and reduces the resistance of heat transfer paths by combining with the optimisation of the flow channel topology to increase the power density of the system from 4.2 kW/L to 10.5 kW/L (a 150% increase) at which is much higher than the traditional solutions (e.g., titanium-grade power supplies with 96% efficiency corresponding to a density of 73 W/in³). This progress provides key technical support for the popularity of GaN in new energy, industrial drives and other high-voltage scenarios [5].

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3.2. Adaptive control

The dual active bridge (DAB) isolation converter employs the adaptive control strategy, the core of which lies in a set of dual-mode driving strategies that can dynamically switch between two operating modes according to real-time operating conditions to optimise the overall performance. The two modes are: Hard Switching Mode and Slow Switching Mode. Hard Switching Mode is mainly used in full load conditions especially when the battery voltage deviates significantly from the optimal matching point or when high power output is required. In this mode, the control system increases the phase shift angle to boost the transmitted power while regulating the primary DC voltage; for schemes using wide-bandgap semiconductors (WBGs) such as Silicon Carbide or Gallium Nitride, peak currents can be further reduced by boosting them appropriately, thanks to their higher voltage withstand capability. The key benefit of this strategy is the significant reduction in switching losses, especially at high switching frequencies, where WBG devices, with their inherent low conduction and low switching losses, can maintain efficiencies of around 99%, much better than silicon devices at lower frequencies. The slow switching mode is designed for light load conditions or capacitive load environments , especially in the early stages of constant current battery charging or when electromagnetic interference (EMI) suppression is required. The core control mechanism of this mode is to limit the peak current by limiting the phase shift angle to prevent the resonant inductor from saturating; for GaN solutions, the gate drive loop is optimised to minimise parasitic inductance to ensure smooth and stable mode switching. The core benefit of this mode is the achievement of softer switching behaviour, manifested as a smooth transition of the switching waveform, which significantly reduces the high-frequency switching noise, with measured results showing that the EMI noise can be reduced by about 18dB . This adaptive dual-mode control strategy, which combines the excellent performance of WBG devices and advanced package integration technology, enables the system to not only simultaneously combine high efficiency and low EMI over a wide input/output battery voltage range, but also significantly increase the power density, improving the power density, system efficiency and reliability of applications such as in-vehicle chargers, and supporting bi-directional energy flow to satisfy the needs of the smart grid [13].

4. Industrial landing and cost

4.1. Manufacturing cost analysis

In the field of power semiconductor devices, cost is a key factor affecting the choice of technology, involving both substrate material cost and process value added. Super-junction silicon (SJ-Si) devices have a significant advantage in cost, thanks to the mature manufacturing process and large-scale production of silicon materials, the cost of its silicon substrate is only 0.1 € /cm². Process value-add includes deep trench etching technology for building superjunction structures, which improves switching performance by optimising the doping region and reducing on-resistance. In single-phase power factor correction (PFC) applications, SJ-Si devices in combination with high-speed switching designs enable low losses and support efficient operation in boundary conduction mode (BCM), competing aggressively with wide-bandwidth devices. In contrast, vertical gallium nitride (GaN) devices have substrate costs of up to 100€/cm² due to their scarcity and high purity requirements. Process value-add involves sapphire hetero integration, which reduces overall cost by growing GaN epitaxials on low-cost silicon substrates, but introduces leakage issues due to threading dislocations, which affects reliability. Although GaN's wide-bandwidth characteristics

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provide 10 times the breakdown field strength of silicon, with theoretical breakdown voltages of up to 2100V, optimisation of structures such as edge termination is required. Through machine learning-assisted TCAD simulation, the design efficiency was improved and a breakdown voltage of 1887V was successfully achieved, highlighting its high voltage potential. Overall, SJ-Si is more affordable for cost-sensitive applications, while vertical GaN is suitable for high-voltage scenarios, but the cost savings of heterogeneous integration need to be balanced with reliability [11,13].

4.2. Technology maturity comparison

There are three key time points in the development history of SJ-Si. In 2000, Infineon CoolMOS™ began mass production of 600V SJ-MOSFETs, breaking through the silicon limit and reducing on-resistance by 10 times compared to traditional devices. In 2010, the yield of the deep trench etching process reached 80%, but etching defect rate of 5.2% became a bottleneck. By 2023, SJ-Si penetration in automotive OBC surpassed 40%, and the Infineon 65R130C7 supports 100V/ns dv/dt. The core vertical GaN industry can be summarised in the following two areas. The first issue is dynamic Ron on degradation issues, where an electron trap activation energy of 0.42 eV reduces device reliability and efficiency due to carrier capture by deep energy level traps, leading to a 70% increase in on-resistance at high temperatures. The second issue involves cost and material defects; the current GaN-on-Si substrate suffers from high dislocation density, which results in increased leakage current. Meanwhile, the cost of GaN-on-GaN substrates remains high, and the lack of maturity in heterogeneous epitaxial technology hinders the ability to scale applications [4,11,13].

5. Conclusion

This review systematically comprehends the technical characteristics of superjunction-on-silicon (SJ-Si) and vertically-structured GaN power devices and their applicability scenarios, with a focus on the optimisation of the comprehensive device performance by the multiphysics-field co-design strategy. The study shows that SJ-Si devices, with their low conduction loss and cost-effective advantages, have occupied a mainstream position in cost-sensitive applications such as consumer electronics and data centre power supply, while vertically-structured GaN devices are more suitable for high-frequency and high power density applications such as new energy automotive electric drive systems and industrial energy conversion, relying on their excellent voltage withstand characteristics and high-frequency performance. The synergistic optimisation of electrical-thermal-mechanical multi-physical fields (including coupling simulation and material interface regulation) can simultaneously improve the conversion efficiency, system robustness and cost-effectiveness of the devices, providing an important basis for the design of the next-generation power systems.

However, this study still has several limitations. First, the experimental validation scope is limited, and some of the simulation models do not cover extreme operating conditions (e.g., ultra-high switching frequency, transient thermal shock, etc.), and the analyses are only based on general operating conditions; second, the study needs to be strengthened and not fully explored; and third, the study is not yet completed. Third, the comprehensiveness of the research needs to be strengthened, and issues such as new packaging materials and system-level electromagnetic compatibility (EMC) have not been fully explored.

Future development in this field should focus on technological breakthroughs and application expansion. Technological advancements include heterogeneous integration innovation, such as developing vertical GaN devices on SiC substrates for ultra-high voltage and low dynamic loss, and optimizing core processes using Atomic Layer Etching (ALE) to enhance gate reliability.

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Application expansion involves short-term goals like promoting GaN modules in new energy vehicle 800V platforms and long-term goals like building a smart grid ecology through integrated energy systems. GaN power devices, driven by the need for "high efficiency" and "low cost," are poised to become a core force in the energy revolution and low-carbon transformation, supporting future social intelligence and electrification.

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