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Current Status and Future Optimization of Low-Power Design in Digital Circuits

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Abstract. The advantages of low power consumption are evident: significantly re ducing system operational costs and facilitating startup conditions. Lowpower design provides a perpetual development goal for circuits, driving continuous efforts to minimize power consumption. This study systematically analyzes the current status and future optimization pathways of low-power design techniques for digital circuits, focusing on two core directions: circuit simplification and hardware innovation. Through literature review and tool experiments (such as Boolean logic optimization using SymPy and Karnaugh map simplification with Logic Friday), the research quantitatively evaluates the effects of multi-level optimization: at the hardware level, employing partitioned multi-supply multi-voltage (MSMV) domains and dynamic voltage and frequency scaling (DVFS) can achieve 30%-50% power reduction, while novel materials (e.g., carbon nanotube transistors) can suppress static power consumption to 0.05pA. The findings indicate that future advancements require integrating AI-driven automation toolchains (such as Q-learning for logic expression optimization) with cross-layer co-design approaches (including in-memory computing and neuromorphic architectures) to break through the "energy wall" limitation. Software tools need to enhance multi-output cooperative optimization capabilities, while hardware innovation should rely on the convergence of AI and materials engineering, ultimately achieving full lifecycle energy efficiency optimization.

Keywords: Digital circuits, Low power consumption, Current status, Circuit design

1. Introduction

In Low-Power Analysis in Digital Integrated Circuits, factors affecting energy consumption in digital ICs are noted to be numerous with relatively complex optimization requirements, which hinders substantial progress in low-power design.[1] Furthermore, in The Application and Optimization of Low-Power Techniques in Digital Circuit Design, Li emphasizes that expanding the application scope and recognition value of digital circuits necessitates in-depth exploration of low-power technologies and continuous optimization of their design applications.[2] This enables the development of more energy-efficient digital circuits to better meet application requirements. Thus, low-power design in digital circuits constitutes a critical research focus in contemporary circuit engineering.

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This study addresses two key questions: What is the current research status of low-power techniques in digital circuits? What are the future development trends? This study systematically proposes a dual-optimization approach for low-power digital circuit design, establishing both theoretical framework and practical guidance to break through the "energy wall" in nanometer-scale processes. Through hardware-software co-innovation, it not only significantly enhances energy efficiency in conventional circuits, but also lays methodological foundations for emerging computing paradigms (e.g., neuromorphic chips and in-memory computing).

The AI-driven logic optimization solutions (such as Q-learning-based automated workflows) and novel material applications (e.g., carbon nanotube transistors) demonstrate cross-disciplinary innovation value. Their ultra-low static power characteristics (achieving 0.05pA-level)[3] will drive technological breakthroughs in low-power scenarios including agricultural sensors and edge computing, carrying strategic significance for realizing green computing under the "Dual Carbon" goals.

2. Research Status Analysis

As IC processes advance to deep submicron/nanometer scales, both static leakage power and dynamic switching power increase significantly. The expansion of chip scales and the increasing complexity in multi-voltage domain management exacerbate power consumption challenges. Therefore, avoiding and simplifying complex high-power circuits becomes particularly crucial.

2.1 Circuit Simplification

Complex circuits often require systematic simplification methods. Standard approaches employ Boolean algebra and Karnaugh map techniques, where any combinational logic circuit can be represented through fundamental AND, OR, and NOT operations. Table 1 presents the content of core Boolean simplification theorems.

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Table 1. Boolean simplification theorems[4]

Theorem	Formula
Combination	$1.\ AB + A\bar{B} = A$
	$1\prime.\ (A + B)\left(A + \bar{B}\right) = A$
Absorption	$2.\ A + AB = A$
	$2\prime.\ A\,(A + B) = A$
	$3.\ A + \bar{A}B = A + B$
	$3\prime.\ A\left(\bar{A} + B\right) = AB$
Redundancy	$4.\ AB + \bar{A}C + BC = AB + \bar{A}C$
	$4\prime.\ (A + B)\left(\bar{A} + C\right)(B + C) = (A + B)\left(\bar{A} + C\right)$
	$5.\ AB + \bar{A}C + BCD = AB + \bar{A}C$
	$5\prime.\ (A + B)\left(\bar{A} + C\right)(B + C + D) = (A + B)\left(\bar{A} + C\right)$
	$6.\ AB + \bar{A}C = AB + \bar{A}C$ (Identity)
	$6\prime.\ (A + B)\left(\bar{A} + C\right) = (A + B)\left(\bar{A} + C\right)$

By expressing circuits as Boolean functions and applying simplification theorems, hardware implementation can be optimized. However, manual computation is error-prone for highly complex circuits. Karnaugh maps (K-maps address this by utilizing Gray-coded arrangements where adjacent cells differ by only one variable. This allows rapid simplification of 2^n contiguous cells using $A+\bar{A}=1$. Tools like Logic Friday implement K-map optimization. Python with SvmPy also enables Boolean simplification from sympy import * from sympy.logic import simplify_logic.

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2.2 Hardware Evolution

Hardware-Software-EDA co-design has become mainstream, enabling full-linkage power control through system-level management (e.g., DVFS) and physical-level optimization (e.g., multi-threshold CMOS).[5]

Table 2. Summary of hardware-level low-power improvements

Level	Core Improvement	Power Reduction
Power Architecture	Partitioned MSMV + DVFS	30-50%
Gate-Level Circuit	Gate Sizing + Asynchronous Design	20-35%
Physical Process	Multi-Vth + 3D Transistor	25-40%
DFT	Low-Power Scan Chain + BIST	40-60%

It can be observed from Table 2 that hardware innovations provide critical trade-offs between component count and processing efficiency, facilitating the design of fast, low-power circuits.

3. Future Development

3.1 Software Enhancement

Existing tools exhibit significant limitations in multi-output optimization. Current solutions (e.g., PyEDA's espresso_exprs) fail to adequately identify shared implicants across outputs, resulting in suboptimal logic reductions. Most commercial tools currently support only single-output functions, necessitating manual intervention for multi-output co-optimization. Proposed improvements include:

AI-guided flow: Small-scale: K-map tools (e.g., Logic Friday); Medium scale: Espresso (PyEDA); Large-scale: Genetic algorithms with versior stability checks,

Automation enhancement: Apply Q-learning to logic optimization reducing literal count by 12% vs.traditional Espresso for 15-variable functions while avoiding local minima

3.2 Hardware Breakthroughs

Novel materials enable radical improvements:

Carbon-based transistors: CNT FETs exhibit leakage currents 1/100th of silicon. Combined with MoS_2's high mobility (12 $cm^2/V \cdot s$), static power reduces by 78% (standby current: 0.05 pA @ -40°C).

Embedded lightweight AI: Agricultural sensors using AI-predicted crop demand models dynamically adjust sampling rates, reducing power by 62% versus fixed-frequency operation.

4. Conclusion

This study systematically explores the current status and future optimization pathways for low-power design in digital circuits, emphasizing two core strategies: circuit simplification and hardware innovation. Through Boolean logic optimization and Karnaugh map techniques, circuit simplification significantly reduces complexity, while hardware advancements—such as partitioned multi-supply multi-voltage (MSMV) domains and dynamic voltage/frequency scaling (DVFS)—achieve 30%–50% power savings. Novel materials like carbon nanotube transistors (CNT FETs) further suppress static power to 0.05 pA, demonstrating the potential for radical improvements in

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energy efficiency. AI-driven automation, particularly Q-learning for logic optimization, enhances traditional methods by reducing literal counts and avoiding local minima. Cross-layer co-design, integrating software tools with hardware innovations, emerges as a critical approach to overcoming the "energy wall" in nanometer-scale processes. These advancements not only enhance conventional circuit performance but also support emerging paradigms like neuromorphic computing and in-memory architectures, aligning with global sustainability goals such as the "Dual Carbon" initiative. This study has three key limitations: AI optimization tools remain theoretically validated, mass production feasibility of new materials like CNT FETs requires verification, and analog circuit low-power design is not addressed. Future priorities include: demonstrating practical effectiveness of AI-EDA tools, resolving manufacturing challenges for carbon-based transistors, and developing system-level frameworks for analog-digital co-optimization. These advancements will accelerate ultra-low-power electronics development, providing critical technological foundations for green computing solutions.

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