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Review of innovations in low-power flip-flops based on the development of innovative logic gates

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Abstract. Integrated circuits have advanced quickly alongside the semiconductor industry's tremendous growth. The primary design considerations for each circuit in a VLSI data path are minimization of area and power consumption. As a very important logic unit in the integrated circuit, reducing the flip-flop's power consumption is of great significance for improving the performance of the whole circuit. There are many ways to reduce the power consumption of the flip-flop. This paper reviews several new low-power flip-flop designs using methods to improve the logic structure of flip-flops and their logic gates, including a reversible flip-flop design with reversible gates, a flip-flop design with memristors, and a sense amplifier-based flip-flop. The analysis shows that all three options for improving the logic gate can reduce the power consumption of the flip-flops and also have a positive effect on reducing the size of the device.

Keywords: flip-flop, reversible logic, low power design, memristor.

1. Introduction

Integrated circuits, due to their high performance, high reliability, high design productivity, low power consumption, and low cost are widely used in all areas of life and production. The demands of today's high-speed data throughput have led to increasing circuit clock frequencies and increasing circuit integration by reducing the feature size of transistors during product development, but the prominent problem of increased power consumption is inevitable. It is therefore a very important area of research today to reduce the power consumption of circuits while maintaining a high level of performance. The flip-flop, a very important component of the integrated circuit, is now used to reduce its power consumption in several ways, including by improving the flip-flop structure, optimizing the clocking scheme, investigating more efficient circuit structures, etc. This paper focuses on some new trigger designs that enhance the trigger structure, such as a reversible flip-flop design with reversible gates, a flip-flop design with memristors, and a sense amplifier-based flip-flop. It describes their logical functions and verifies their low-power characteristics in comparison with conventional flip-flops. It also describes the current state of research on enhancing logic gates to lower flip-flop power consumption.

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2. A reversible flip-flop design with reversible gates

Landauer emphasizes that the irreversible operation of current logic circuits is the source of energy consumption. And that the key to reducing power consumption in circuits is to convert irreversible operation to reversible operation [1]. Reversible computing is an important research direction for future low-power integrated circuits because it eliminates energy dissipation due to data loss in traditional logic circuits. Using reversible logic gates to build reversible circuits can effectively reduce computational energy consumption [2].

The main reversible logic gates used in reversible logic networks are NOT gates, Feynman gates, Swap gates, Fredkin gates, and Toffoli gates. In the following design of the reversible flip-flop, the Fredkin gate, the Modified Fredkin gate, and the Feynman gate are mainly used.

Fredkin gates and Modified Fredkin gates are both three input/output gates. Yet their quantum costs are 5 and 4 respectively. This means that if the MF gate can be used instead of the F gate as much as possible, this will significantly reduce energy consumption [3].

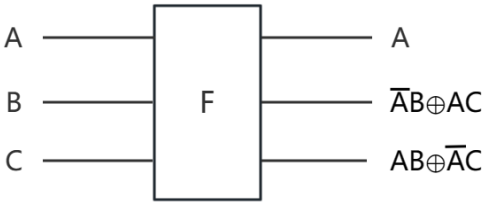

Figure 1. Fredkin gate.

Its function is described as follows: As is shown in Figure 1 that when A is 1, the output of control bit A remains unchanged, and the outputs of target bits B and C are exchanged. When A is 0, neither the control bit A nor the target bits B and C change. When A is 0, neither control bit A nor target bits B and C are changed.

Change the second output of the F gate to $\overline{A}B \oplus A\overline{C}$, and then the modified fredkin gate (MF gate) can be obtained. Its function is described as follows.: when A is 1, the control bit A is unchanged, the outputs of target bits B and C are swapped, and the target bit C is inverted. When A is 0, both control signal bit A and target bits B and C are unchanged.

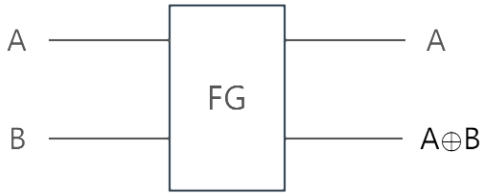

Figure 2. Feynman gate.

Feynman gate is a two input/output gate. Its function is described as follows: As is shown in Figure 2 that when A is 1, the control bit A is output, which is unchanged and the target bit B is inverted; when A is 0, the outputs of both the control and target bits remain unchanged. It can be used to perform inverse and copy operations on signals.

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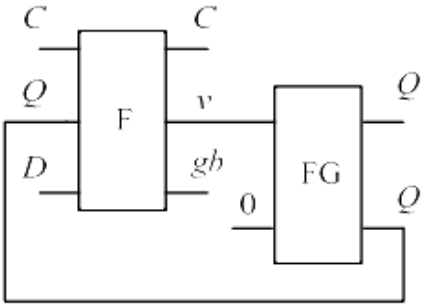

Figure 3. D latch implemented with F gate and FG gate [3].

Figure 3 displays a high-level triggered D latch implemented with an F gate and an FG gate. When C is 0, v = Q, gb = D, in this case, the FG gate copy function enables a loop between the circuit output and the input forming a loop. When C is 1, the F-gate is in the data exchange state, v = D, which causes the output signal of the FG gate to change to D, enabling the update of the data. And a level-triggered reversible D flip-flop with a smaller quantum cost can be obtained by replacing the Fredkin gate with a Modified Fredkin gate with a smaller quantum cost [4].

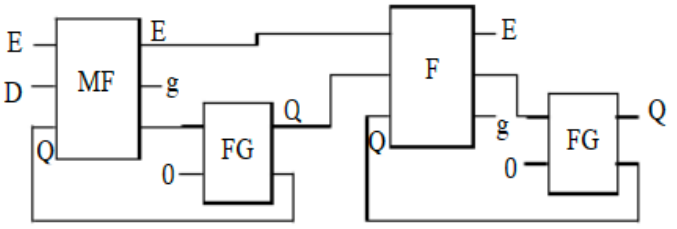

Figure 4. Master-slave D-FF using F, MF and FG gates [4].

Figure 4 shows a master-slave D-FF using F, MF and FG gates. When E = 1, then master FF will work, and when E = 0, slave FF will work. If this research uses the MF gate instead of the F gate, then the quantum cost will be lower. This completes the design of the flip-flop using reversible logic devices.

3. A flip-flop design with memristors

As semiconductor technology advances at a rapid pace, Moore's Law, which was once a great authority, is being challenged [4]. The memristor is the fourth passive basic circuit component with the advantages of low power consumption, non-volatility, and high density. Circuits constructed using memristors can effectively break through bottlenecks, reduce the number of components, and energy consumption, maintain the original efficiency of the circuit. This new device was first proposed in 1971 and created in 2008 [6, 7]. In a bipolar memristor, the resistance of the memristor increases when the current flows in one of the directions, while the resistance increases when the current flows in the opposite direction decreases. Great efforts have been made by previous researchers in the construction of logic circuits using memristors, including material implication [8, 9], memristor-aided logic [10], Reconfigurable non-volatile logic gate circuits [11], and so on. The focus here is to design a D flip-flop based on the reconfigurable non-volatile logic gates [12].

This design was completed using MRL——a hybrid CMOS-memristive logic family [13].In this logic family, the high level (VH) represents logic '1', and the low level (VL) represents logic '0'.

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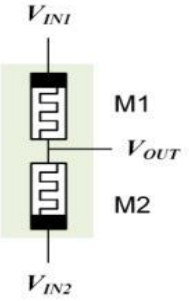

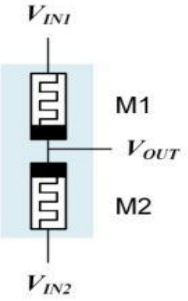

Figure 5. AND gate [12]. **Figure 6.** OR gate [12].

Figure 5 shows the and gate constructed by MRL,and figure 6 shows the or gate. In the following analysis of the memristor, this study uses 'M' to denote its resistance value. Meanwhile, this study takes the example of a logic analysis of and gate. When both inputs are high or both are low, there is no current flow in both memristors and therefore the output level is the same as the output level. And when the input levels of the two inputs are reversed, for example, V_{IN1} inputs at high level and V_{IN2} inputs at low level. When the input levels of the two inputs are reversed, M1 will approach the maximum resistance and M2 will approach the minimum resistance, according to the characteristics of the memristor. The formula below can be adopted to calculate the output voltage.

$$V_{OUT} = \frac{M2}{M1+M2} V_{IN1} \tag{1}$$

M2 is much smaller than M1, so the value of the output voltage tends to 0. The situation is similar when the inputs of the two memristors are reversed, again outputting 0.

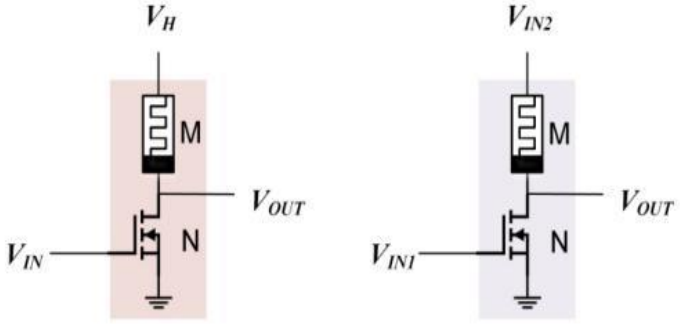

Figure 7. NOT gate and its extension [12].

Figure 7 displays a NOT gate and its extension. Similar to the previous gate, an expression for the output voltage can be easily obtained.

$$V_{OUT} = \frac{M}{M+R_N} V_H \tag{2}$$

In this expression, R_N represents the resistance of that NMOS transistor. When the input goes high, NMOS is on, the output voltage is grounded and it has a value of 0. Conversely, if the input is low, NMOS transistor does not conduct and its resistance tends to infinity. Then V_{OUT} is equal to V_H and the output is high. The study can extend this circuit by replacing V_H with V_{IN2} to obtain a logical expression like this.

$$V_{OUT} = \overline{V_{IN1}} * V_{IN2} \tag{3}$$

In formula (3), the asterisk (*) represents the 'and' operation.

After introducing these gates, a D flip-flop design can be started. The equation of state for a D flip-flop is as follows(level triggered).

$$Q_{N+1} = CD + \overline{C}Q_N \tag{4}$$

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C indicates the clock signal, and D and Q indicate the input and output signals. From the equation of state, it follows that when the clock is at a low level, $Q_{N+1}=Q_N$, the output signal remains constant. Conversely, Q_{N+1}=D. It is important to note that, in the presence of a specific applied current or voltage signal, the resistance of the memristor can be switched between at least two stable resistance states (high and low resistance) and remain constant after the applied electrical signal is removed. Therefore, it is necessary to analyze the situation corresponding to the different outputs of the previous moment. When Q_N=1, $Q_{N+1}=CD+\overline{C}$, and when Q_N=0, $Q_{N+1} = CD$. This can be achieved by means of the above-mentioned and gate, or gate and modified not gate.

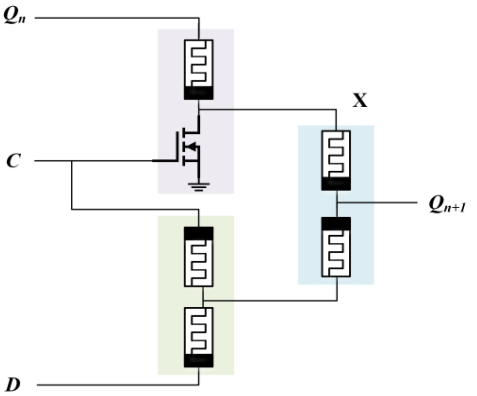

Figure 8. D flip-flop based on MRL [12].

A D flip-flop implemented using memristors is shown in Fig8. When Q_N inputs logic 0, X outputs logic 0. Then after passing through the or gate, Q_{N+1} = CD+X = CD can be got. For the same reason, when Q_N inputs logic 1, $Q_{N+1}=CD+\overline{C}$ can be obtained. So far, a D flip-flop has been designed based on memristor ratioed logic. It can be seen that though the number of devices is the same for a design using a memristor compared to a conventional D flip-flop, the device area is much smaller than a pure CMOS structure. Using a similar approach, this study can also design a JK flip-flop based on the MRL, which can save up to 60.58% of power consumption [12], achieving the goal of designing a low-power flip-flop.

4. Sense amplifier based flip-flop

Flip flops form an important part of the overall circuit design, one of the most effective flip-flops is the Sense Amplifier based Flip-Flop (SAFF) [14]. In the area of high speed and low power performance, a wide range of SAFF designs are preferred by researchers The potential for portable, high computing and low power consumption is very promising. This section focuses on an improved SAFF design from the perspective of the flip-flop's low power consumption.

Masataka Matsui gives the first design of SAFF, as is shown in Figure 9 [15].

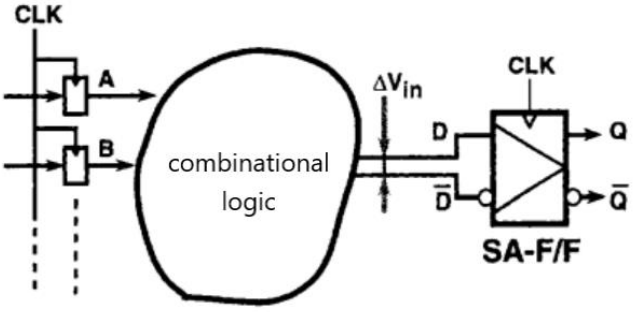

Figure 9. SAFF basic block diagram [15].

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The SAFF consists of two parts, a SenseAmplifier (SA) master stage and a slave stage with a reset SR latch.SA) master stage and a slave stage with a reset SR latch. Based on this structure, a restacked adaptive regulation sensitive amplifier and a single-ended output SR latch are proposed [16].

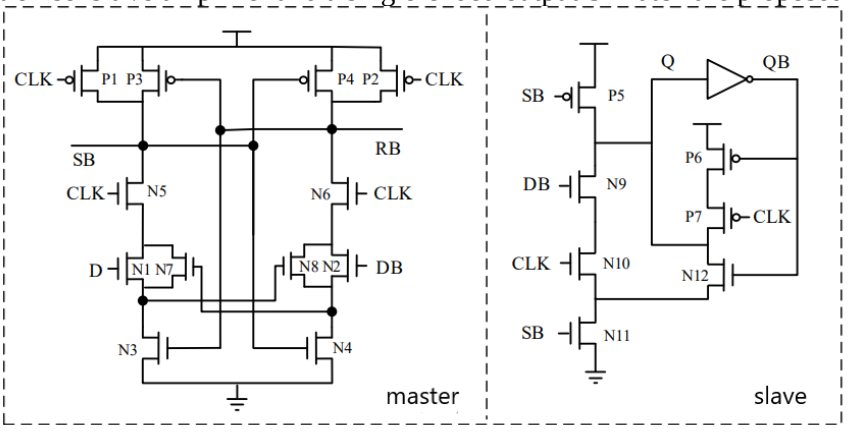

Figure 10. The proposed re-stack adaptive adjustment of single-end output SAFF [16].

Fig.10 displays the proposed re-stack adaptive adjustment of single-end output SAFF. Its function can be divided into three stages.

Stage (1): Input CLK low level, p1 and p2 transistors are turned on, SB and RB precharge VDD high voltage through P1 and P2 transistors, N5 and N6 are turned off. Then N3 and N4 are turned on, N7 and N8 are turned off, and the pre-charging step is completed.

Stage (2): When the rising edge of the clock arrives and makes CLK go high, which results in the cut-off of p1 and p2 while N5 and N6 are on. If D is high, junction SB discharges to low via N5, N1 and N3, simultaneously turning P3 on and N4 off. If D is low, junction RB is discharged low via transistors N6, N2 and N4, simultaneously turning P4 on and N3 off. This completes the induction phase, where a change in D no longer affects the state of junctions SB and RB due to the modulating effect of N7 and N8.

Stage (3): Next, this study analyzes the slave section. If D is high at the rising edge of the clock, SB discharge goes low, as seen in stage 2, causing P5 to conduct and N9, N10, and N11 to cut off. At this point, Q goes high. If D is low on the rising edge of the clock, SB remains high and P5 turns off while N9, N10, N11 conduct, at which point Q is grounded and goes low. When the clock is low, as can be seen from stage 1, SB and RB are held high, the P5, P9, and N10 transistors are cut off, and the Q and QB signals are latched.

At this point, this research has completed the design of re-stack adaptive adjustment of single-end output SAFF. Conventional sense amplifier based flip-flop (Con SAFF) is one of the most efficient low-power flip-flops available [17]. The new SAFF offers an average power saving of 26% compared to the Con SAFF, including a 32% saving at α (switching activity) = 12.5%, a 46% reduction in clock-to-output latency, and an average reduction of approximately 3 times in power delay product for different process angles and different input data switching frequencies [16].

5. Conclusion

In several of the flip-flops described in this article, flip-flops based on reversible logic gate construction, replacing F gates with MF gates, can effectively reduce the quantum cost and reduce energy consumption. The flip-flop constructed using a memristor has been proven to consume significantly less energy than conventional flip-flops and occupies a smaller area in the chip, SAFF has a short set-up time and hold time, which greatly reduces its clock load. All three of these flip flops use new devices to achieve what traditional CMOS flip flops do. but unfortunately, it is difficult to make a side-by-side comparison of energy consumption because the fields are different. There are many ways to reduce the power consumption of flip-flops, and in the future, efforts can be made to

combine new flip-flops with optimized clock technology and improved semiconductor processes to design low-power, high-performance large-scale integrated circuits.

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