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Progress in the suppression of short-channel effects: Materials and structure

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Abstract. With the rapid development of integrated circuit (IC) technology, the size of devices has been continuously shrinking. While this trend has led to increased integration density, improved device reliability, and reduced costs, it has also resulted in performance degradation of metal-oxide-semiconductor field-effect transistors (MOSFETs) due to the short channel effect (SCE). This paper provides a comprehensive review of the most recent techniques that can mitigate the short channel effect in MOSFETs, with a focus on semiconductor materials and device structures. These techniques include decades-long advancements in doping and high-κ dielectric materials, as well as emerging structures such as Fin field-effect transistors (FinFETs), Gate-all-around field-effect transistors (GAAFETs), Forksheet field-effect transistors, and complementary field-effect transistors (CFETs). This paper can greatly assist researchers in establishing a theoretical foundation, identifying research problems and voids, and identifying hot spots and trends in short channel effect research through a comprehensive analysis of the existing research literature.

Keywords: short-channel effects, doping, high-κ dielectric materials, FinFET, GAAFET, CFET.

1. Introduction

MOSFETs are ubiquitous semiconductor devices that are extensively employed in modern electronic circuits and systems. In the initial stages of development, Gordon Moore, founding members of Intel Corporation, predicted that the total amount of transistors integrated into a semiconductor device would grow by twice annually [1]. In 1965, he revised this prediction to doubling every 18 months, along with a corresponding improvement in circuit performance. Since 1975, the development of CMOS circuits has largely adhered to this trend. With the advancement of technology, MOSFETs have achieved tremendous progress. The integration density of MOSFETs has evolved from tens of transistors on a single chip in the past to over a billion transistors on a single chip today. The characteristic size of the devices has also shrunk from the micrometer scale in the 1970s to the nanometer scale in modern times. Reducing the size of transistors not only increases integration density and enhances operational speed, but also achieves the goals of reducing power consumption and lowering manufacturing costs.

Nonetheless, as transistor dimensions continue to decrease in pursuit of higher performance and integration density, the short channel effect has arisen as a critical challenge that affects device characteristics and reliability. The short channel effect is the phenomenon that occurs when the drain's impact on the channel region intensifies as the length of the channel is reduced to sub-micron or

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nanometer dimensions, causing the transistor's behaviour to deviate from its ideal characteristics. The reason is that when the channel length is similar to the depletion region that resulted from the drain voltage, the electric field within the drain extremity of the channel strengthens, leading to a higher concentration of electric field lines and a higher electric field gradient. This stronger electric field induces higher carrier velocities and accelerates carrier transport towards the channel's discharge end. This results in a number of consequences, such as drain-induced barrier lowering (DIBL), velocity saturation, hot carrier effects and the change of threshold voltage and subthreshold slope. This diminishes the device's performance and renders it unfit for extremely scaled equipment [2]. Hence, comprehending and mitigating the short channel effect has become a top priority in the research and development of field-effect transistors, as it greatly impacts the performance, power consumption, and reliability of the devices.

This paper presents a comprehensive review of the most recent techniques for mitigating the short channel effect in field-effect transistors. These techniques include both material-related optimization approaches, such as doping and high-κ materials, and device structure-related optimization approaches, such as FinFET, GAAFET, Forksheet FET, and CFET. The primary objective is to mitigate the detrimental effects of short channel effect on the performance and reliability of field-effect transistors, while also shedding light on their practical applications and possible future directions.

2. Optimization of materials

2.1. Doping

By preventing the diffusion of source as well as drain depletion layers, increasing the channel-doping concentration typically controls short-channel effects [3]. According to recent research, 2H-phase (semiconducting) transition metal dichalcogenides (TMDs) have the potential to be converted to 1T-phase (metallic) TMDs via chemical alteration [4]. Due to the reduced Schottky barrier height of in-plane contacts and the stronger contact coupling in in-plane connections, in-plane 1T-2H-1T heterojunction of TMDs is utilized to manufacture low resistance contact transistors. The in-plane WTe_2 Schottky barrier field-effect transistors (SBFETs) with a 1T-2H-1T phase configuration, as outlined in the aforementioned theoretical framework, demonstrated remarkable performance when implemented with a channel length of 6.1 nm [5]. Nonetheless, upon reducing the channel length to 5.1 nm, the leakage current surpasses the I_{OFF} value of 0.1 μA/μm, indicating that the in-plane WTe_2 SBFETs with a 1T-2H-1T phase configuration exhibit a limited ability to effectively suppress short-channel effects. Liuming Dou and his research team employed atomic substitution to replace a portion of the tungsten (W) atoms in 2H-WTe_2 close to the source electrode with molybdenum (Mo) atoms. Subsequently, they utilized the first-principles software package Quantum ATK for simulation purposes. The outcomes revealed a decrease in leakage current for the 5.1 nm in-plane WTe_2 SBFETs as the Mo doping number progressively increased. For instance, when Mo doping reached six periods, the minimum current attained 0.053 μA/μm, fulfilling the I_{OFF} requirement of 0.1 μA/μm [6].

2.2. High-κ materials

In accordance with the scaling law, it is essential to consistently decrease the equivalent oxide thickness (EOT) of the gate dielectric to enhance gate control capabilities, thereby satisfying the demands for the ongoing advancement of future transistor technology. As the thickness of the purely thermally grown SiO_2 decreases, the gate leakage current due to the tunneling effect increases exponentially. In this case, the thickness of oxide layer (t_{ox}) of the gate SiO_2 can only be limited to 3 nm to 2 nm and there is no way to sustain the development of technology generations below 45 nm. One approach that has proven to be very effective is to use high-κ dielectrics to replace conventional SiO_2 dielectrics.

Shashi K. Dargar et al. designed the Carbon Nanotube Metal Oxide Semiconductor Field Effect Transistor (CNT-MOSFET) in double-gated structure, and used electronic simulator to analyze the impact of various high-κ gate dielectric materials such as Al_2O_3 and HfO_2 on the characteristics of double-gate structure CNT-MOSFETs. Simulation results demonstrated that when the gate dielectric

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material was the high-κ dielectric material HfO_2 (K = 25), the threshold voltage (V_{TH}), DIBL and ON-OFF current ratio (I_{ON} /I_{OFF}) obtained were 0.397 V, 56.22 mV/V and 3.5×10^5, which were much higher than the threshold voltage of 0.187 V, DIBL of 102.2 mV/V and the ON-OFF current ratio (I_{ON} /I_{OFF}) of 2.3×10^5 for SiO_2 [7].

Another way to significantly suppress the short-channel effect is to place high-κ spacers on both sides of the gate. Gaurav Dhiman and his team from DIT University designed double-gate junction less field-effect transistors (JLFETs) with high-κ spacers and used ATLAS to analyze the effect of HfO_2 and Al_2O_3 spacers made from high dielectric constant materials on the electrical properties of the JLFETs. They found that the threshold voltage (V_{TH}) of the HfO_2 spacer-based JLFET was approximately 0.18 V at a channel length of 22 nm, which is six times higher than the threshold voltage (V_{TH}) of 0.03 V for the SiO_2 spacer-based JLFET. In addition, the DIBL of HfO_2-based devices was three times higher than that of SiO_2-based devices. Last but not least, the I_{OFF} of the HfO_2-based JLFET was lower, which resulted in the ON-OFF current ratio (I_{ON} /I_{OFF}) of 10^6, much higher than that of a normal JLFET [8].

3. Optimization of device structure

3.1. FinFET

As planar MOSFET processes continue to evolve, the short-channel effect severely affects the performance of planar MOSFET devices when the channel length approaches 22 nm, which means that the development of conventional planar MOSFETs has encountered significant difficulties. Therefore, in order to enhance the gate control of carriers in the channel, many research teams have shifted their focus to multi-gate field effect transistors with a three-dimensional structure, one of which is the FinFET. Deviant from conventional MOSFET architectures, FinFETs showcase vertically-oriented channels on the substrate, bearing a resemblance to the fins of a fish. Owing to the gate configuration that encapsulates the channel on three sides, FinFETs offer a superior mitigation of short-channel effects.

Qingzhu Zhang et al. have devised a fin-on-insulator (FOI) FinFET architecture incorporating metal source and drain (MSD) and an HKMG-last process. In comparison to traditional bulk FinFET structures employing p-n junctions, the leakage current of MSD FOI FinFETs witnessed a tenfold reduction at a gate length (Lg) of 20 nm. Furthermore, the MSD FOI FinFET demonstrated enhanced control over short channel effects, exhibiting approximately ~47% DIBL and ~32% SS reductions for 20-nm-Lg PMOS devices. Additionally, the drive current of the 20-nm-Lg MSD FOI FinFET experienced a substantial augmentation with the comprehensive Ni (5% PT) silicide process, reaching up to 547 μA/μm for NMOS and 324 μA/μm for PMOS at VDD = 0.8 V [9]. Zhaozhao Zhang et al. have successfully developed an excellent performance Negative-capacitance (NC) FinFET based on a back-gate FinFET integration process combined with 3-nm-thick ferroelectric (FE) hafnium zirconium oxides ($Hf_{0.5}Zr_{0.5}O_2$) layer. This device achieved a 500 nm gate length NC-FinFET device with subthreshold swing and hysteresis voltage of 34.5 mV/dec and 9 mV respectively, and a 20 nm gate length NC-FinFET device with subthreshold swing and hysteresis voltage of 53 mV/dec and 40 mV respectively, as well as a 260% driving current enhancement [10]. Pin Su et al. investigated and compared the short-channel effects of InGaAs NC and Si NC-FinFETs using a theoretical model confirmed with TCAD numerical simulations, based on existing Ultra-thin-body InGaAs NC-FET structures. The results showed that the short-channel effect of InGaAs NC-FinFETs can be significantly improved with the presence of negative capacitance effects [11]. V. Bharath Sreenivasulu et al. invoked $Hf_xTi_{1-x}O_2$ high-κ dielectric gate stack and optimized usage of spacer on the basis of an existing silicon ultrathin junction less FinFET. In this way, the electrical characteristics of the device were analyzed at channel lengths of 1 nm and 3 nm. The results indicated that the application of the spacer technique successfully reduced the OFF current from ~10^{-9} A/μm to ~10^{-13} A/μm. In addition, the I_{ON}/I_{OFF} ratio reached ~10^{-9} at trench lengths of 1 nm and 3 nm [12].

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3.2. GAAFET

As the FinFET pitch between the two gates is further reduced and the fin height continues to increase, this leads to problems such as high parasitic capacitance and significant short channel effect. However, GAAFET exhibits a gate configuration that encapsulates the channel from all four sides, thereby offering superior gate control as compared to the FinFET design, which features a three-sided gate envelopment of the channel. This demonstrates that GAAFET has an advantage in the development of sub-3 nm technology nodes and is better able to meet the technical challenges mentioned above. Therefore, the development of integrated circuits below the 3 nm technology node is the stage of transition from FinFET to GAAFET. At the same time as the size of FinFET evolved from 10 nm to 7 nm, different GAAFET structures have been investigated, both lateral and vertical for channel orientation, or nanowires (NWs) and nanosheets (NSHs) for channel structure.

H. Mertens et al. fabricated GAA n-MOSFETs and p-MOSFETs with vertically stacked horizontal silicon nanowires of 8 nm diameter on a bulk silicon substrate based on the replacement metal gate process. This device had very high electrical characteristics: the SS is 65mV/decade and the DIBL is 42 mV/V at Lg = 24 nm [13]. In 2017, N. Loubet et al. prepared for the first time a horizontally stacked GAA nanosheet structure with Lg = 12 nm and a contacted poly pitch (CPP) of 44/48 nm for use sub-5 nm technology nodes. Thanks to the large effective width (Weff), it had excellent short-channel characteristics: at Lg = 12 nm and CPP = 44 nm, the n-FET has an SS of 75 mV/decade and a DIBL of 32 mV/V, and the p-FET has an SS of 85 mV/decade and a DIBL of 24 mV/V [14].

As the move to smaller processes continues in the future, there will be a requirement for smaller spacing between NMOS and PMOS devices in standard cells, whereas the FinFET and GAA NSHs processes limit this reduction of spacing. To address this problem, IMEC first proposed fork architecture in the SRAM scaling research published by IEDM in 2017. This structure allows the Gate Extension over active fin (GE) on one side of the device to be removed completely and the edges of the gate to be self-aligned with the device without additional complex steps. Despite the fact that the forksheet structure exhibits diminished channel controllability in the z-direction when contrasted with a conventional GAA configuration, resulting in a reduction of its electrostatic control capability, the area of SRAM bit cell using this structure will be reduced by 20% and performance improved by 30% at technology nodes beyond 5 nm [15].

In 2019, the forksheet architecture was unveiled as the optimal logic scalability solution for the 2 nm node. This innovative structure unifies NMOS and PMOS within the same framework. A dielectric wall is introduced to technically divide the P-gate trench from the N-gate trench. When compared to GAA nanosheet devices of equivalent size and form factor, the forksheet structure achieves a reduction in subthreshold slope (SS) of 4 mV/dec at saturation, with sheet widths and thicknesses measuring 13 nm and 5 nm, respectively. This leads to an 18% degradation in I_{on} for the same I_{OFF} value of 10^{-9} A. In addition, the forksheet structure operates at a 10% higher frequency and consumes 24% less power than the GAA nanosheet structure at the same power level, and has a 20% smaller area [16].

In 2022, H. Mertens et al. from IMEC presented a 10 nm forksheet FET structure featuring a dielectric wall width, employing a bottom dielectric isolation (BDI) layer. This layer was achieved by substituting the SiGe epitaxial layer with a dielectric film, which served to isolate the transistor from the substrate. Based on this innovative architecture, the drain-bulk current levels measured in forward bias for the BDI device were found to be orders of magnitude lower than those observed in devices lacking BDI, reaching the experimental noise level [17].

The technical architecture of the forksheet is not perfect either. In this structure, the gate does not completely surround the channel due to the presence of the dielectric wall, so the channel control is slightly reduced. To solve the electrostatic control problem of the Forksheet, the CFET was then born.

In 2018, Imec spearheaded the development of the complementary FET (CFET) structure and assessed its performance through the lens of design-technology co-optimization (DTCO) methodology. This innovative architecture is achieved by stacking an n-type vertical sheet atop a p-type fin. This CFET allows for a 50% reduction in the size of the structures of the standard cells and SARMs provided. To meet the 3 nm target, Imec's proposed CFET structure reduces the parasitic resistance of deep vias by

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introducing advanced MOL contacts with thin barriers. Also, because the gate of the CFET operates orthogonally to the contact, the CFET minimizes the parallel capacitance of the gate and drain and the extension of the gate beyond the fin, which in turn leads to a reduction in Miller capacitance. Based on TCAD's analysis, it is clear that as expansion is reduced to 10 nm, the power and performance of CFETs are superior to that of FinFETs and the performance requirements of the 3 nm target can be achieved [18].

In 2022 Yanna Luo et al. proposed an architectural design and integration scheme for Novel Hybrid Channel Complementary FETs (HC-CFETs) utilising a vertical structure, and used the industry's mainstream Design-Technology Co-optimization (DTCO) methodology to fully explore the advantages of this new hybrid channel CFET's architecture. The structure facilitates the co-optimization of the desired high electron and hole mobility surfaces of NMOS and PMOS on a singular substrate, without relying on hybrid crystal orientation techniques such as wafer bonding. The HC-CFET structure provides the flexibility to seamlessly integrate nanowires and nanosheets, allowing for NMOS devices with a (100) channel surface orientation, as well as PMOS devices with a (110) channel surface orientation. On the basis of this optimization of the channel surface direction, the current gain of NMOS and PMOS is capable of being increased by about 20% instead of diminishing the SS and DIBL characteristics. Therefore, the short channel effect is unaffected by the rise in drive current caused by the optimization of the channel surface direction. The results indicated that the preferred method for producing HC-CFET is to utilize a (110) wafer with an n-type nanowire (n-NW) layer positioned atop a p-type nanosheet (p-NS) stack. And this device exhibits superior performance and structural functionality in this circumstance [19].

In December 2022, Peng Zhou et al. innovatively proposed a heterogeneous CFET structure, which integrated wafer-scale silicon-on-insulator p-type FETs and molybdenum disulfide (MoS_2) n-type FETs. Experiment results proved that the intermediate common gate had an excellent control of n-type (MoS_2) and p-type (p^--Si) transistors. As the voltage at the common gate changed from -4 V to +3 V, the drain current of the MoS_2 nFET experienced an increase from approximately 1 pA to 3.43 μA, while the drain current of the SOI pFET saw a reduction from 31.7 μA to 45 pA. The I_{ON}/I_{OFF} of the nFET and pFET were approximately 3.43×10^6 and 7.04×10^5 respectively, with subthreshold swings of approximately 160.4 mV/decade and 147.8 mV/decade correspondingly. Simultaneously, the electron mobility of MoS_2 is comparable to the hole mobility of silicon, resulting in an excellent device performance match. For instance, the inverter gain reaches up to 142.3 at a power source voltage of 3 V, while exhibiting a gain of 1.2 at an ultra-low voltage supply of 0.1 V, accompanied by a low power consumption of merely 64 pW. The approach successfully creates a 4-inch large-scale three-dimensional heterogeneously integrated complementary field-effect transistor by integrating the novel two-dimensional material MoS_2 on a silicon-based device using the tried-and-true back-end procedure [20].

4. Conclusion

This article discusses advanced mitigation techniques in detail, including material optimization and device structure optimization. These methods aim to mitigate the adverse impacts of short-channel effects on the performance and reliability of FETs, while their practical applicability and potential future directions are discussed in depth. As device sizes continue to shrink, the scaling of conventional planar MOSFETs has reached a bottleneck despite optimizations in material aspects such as doping and high-κ materials. The development of integrated circuits has now entered the era of nanoelectronics with FinFET and GAAFET technologies, where combined optimizations in materials and device structure have led to superior size and performance characteristics of new FinFET and GAAFET devices, including forksheet FET and CFET, among others. Further research in this area is essential to overcome the challenges posed by the short-channel effect and to enable continued advances in field-effect transistor technology in the nano-electronic era.

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