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# Overcoming sub-threshold slope degradation by the advances of TFETSs materials

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**Abstract.** With the scaling of devices in the past few decades, a lot of problems arise include short tunnel effect and significant power consumption, in which sub-threshold slope is a considerate factor. However, Sub-threshold Slope of MOSFET is limited to 60 mV/decade at room temperature due to "Boltzmann Tyranny". TFETs (Tunnelling Field Effect Transistors) are the most promising field-effect transistors candidates owing to its potential to overcome sub-threshold slope degradation. This article illustrates the main principles of TFETs and explains how TFETs can overcome sub-threshold slope degradation through tunnelling effect. Furthermore, this article introduces the advances of TFETs materials to optimize devices performances.

**Keywords:** subthreshold slope; TFETs; material system.

## 1. Introduction

Ever since the transistor was invented, the size of transistors has been shrinking under the push of Moore's law which means over an 18-month period, the number of transistors that an integrated circuit can accommodate doubles. The smaller the transistor, the more transistors there can be in an integrated circuit of the same size, and the more parallelism and logic the integrated circuit will have. In short, if the critical size of transistors can be further reduced, our electronic products can be more portable, versatile and powerful.

However, with the scaling of transistors and enters the size of nanometer, the scaling behavior arises a lot of problems, such as reducing reliability of transistors, short-channel effect, increasing the leakage current and arising of the design and production costs. Also, the Dennard Scaling Principle seems to have failed. The Dennard Scaling Principle means as transistors get smaller and smaller, their power density stays the same, so power consumption is proportional to area and the magnitude of voltage and current is proportional to their length. However, when the chip size stays the same and the number of transistors increases, the current leakage will cause the chip to heat up, and further causing energy

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consumption and thermal problems. In spite of that, due to the limitation of Boltzmann tyranny, the operation voltage ($V_{DD}$) of the MOSFETs cannot be scaled down in proportion to device size0. In today's integrated context, if more transistors are packed into the same size area because of the transistors' scaling, but the power of the transistors remains high, the energy consumption will be unacceptably high. As a result, the power consumption of the FETs (Field Effect Transistors) becomes one of the serious problems which hinder development of transistors.

The power consumption of the FETs is relative to the $I_{on}$ (on-state current), $I_{off}$ (off-state current), the ratio of $I_{on}$ and $I_{off}$, the static power consumption and the sub-threshold slope (SS). In order to obtain a low power consumption, we need to acquire low on-state current, high ratio of $I_{on}$ and $I_{off}$ and a steep sub-threshold slope. This thesis will focus on getting a steep sub-threshold slope.

However, the SS of the traditional MOSFETs is usually located at the range between 80-120 mV/decade. Also, because of its performance characteristic which is based on HCE (Hot Carrier Effect), the minimum SS can't break through the limitation of 60 mV/decade. So, we need new technology and material to keep decreasing the SS. Tunnelling Field Effect Transistors (TFETs) is a potential solution. TFET devices work through the tunnelling of carriers, so the HCE has almost no influence on TFET, which avoids the problems of large power consumption and allows the SS breaking 60 mV/decade limitation [2]. What's more, the characteristic of TFETs determine the smaller the size, the more obvious tunnelling effect will become, which on the contrary improve the performance of TFET. All the advantages mentioned above enable the TFETs a possible solution for the future. But if we wish to further reduce the SS of TFETs and improve its performance, we will need to replace the Silicon base with new materials.

## 2. Subthreshold slope

### *2.1. Subthreshold state information*

The transistor subthreshold state is a focus of people studying transistors, and it is itself an important operating state of MOSFETs. It is itself also called by people as MOSFET subthreshold region and is the premise of the research of this piece of paper. This is a state where the gate voltage $V_{gs}$ of the MOSFET is below the threshold voltage $V_T$, and there is no conducting channel below an operating state, and there is no conducting channel, i.e., a state where $V_{gs} \leq V_T$ , surface potential $\psi_s \approx$ Fermi potential $\psi_b$ (i.e., the surface is weakly inverse). At this time there is still a smaller current through the device, the electricity is still a smaller current through the device, the current is called sub-threshold current. The subthreshold current is relatively small, but this also accomplishes a bit of it, that is, it is easily controlled by the gate voltage, so the subthreshold state of the MOSFET is ideal for low voltage, low power consumption operation, this way is very favorable. This characteristic also makes it very popular and valued by scientists in large-scale integrated circuit applications such as logic block tubes and storage again.

### *2.2. Subthreshold characteristics*

Since the surface potential $\psi_s = V_{gs} - V_T$ , the subthreshold current of the MOSFET is $I_{dsub} \propto \exp(q\psi_s/kT) \propto \exp(q [V_{gs} - V_T] / kT)$, i.e., the output subthreshold current increases exponentially with the input gate subthreshold gate-source voltage source voltage $V_{gs}$; and at $V_{ds} >$ 3kT/q, the subthreshold current has little relationship with $V_{ds}$. However, at $V_{gs} > V_T$ (i.e., $\psi_s > 2\psi_{fb}$, i.e., trench), there is a linear or squared relationship between the output source drain current and $V_{gs}$, which is normal and has a linear or squared relationship between the MOSFET conductive currents, which is normal. Applications have great value. Therefore, in the ultra-large-scale integrated circuits ultra-large-scale integrated circuits, although the basic device used is the MOSFET, but the physical basis of its work is the bipolar transistor principle. Performance indicators that measure the subthreshold state are the subthreshold slope as well as the subthreshold swing.

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Subthreshold slope is a characteristic of MOSFET current-voltage. In the subthreshold region, the decreasing forward-biased diode current was resembled exponentially by the drain current behavior (although the gate terminal controls it). Thus, with fixed drain, source and body voltages, the drain current versus gate voltage plot will exhibit approximately log-linear behavior for this MOSFET operating state. This kind of operating state in MOSFET is called subthreshold slope. The subthreshold swing is a performance indicator that measures the mutual transition rate between the on, off states of the transistor, which represents the amount of change in gate voltage required for a tenfold change in source-drain current, and a smaller S means that the on/off rate ON/OFF is faster. At present, the limit value of SS at room temperature is about 60mV/dec, and it is difficult to reduce with the reduction of device size [3, 4].

### *2.3. Formula explanation*

The formula of subthreshold swing is shown as Eqn (1) and Eqn (2). where $\varphi_S$ is the surface potential and $I_D$ is the leakage current. The first term m indicates the ability of $V_{GS}$ to modulate the surface potential $\varphi_S$. The smaller the *m*, the stronger the gate modulation of the channel, and vice versa, the weaker. *m* depends on the gate structure and dielectric material. The second term *n* represents the amount of surface potential change required to raise the current $I_D$ by one order of magnitude, and its magnitude depends on the current conduction mechanism [5].

$$\mathrm{SS} = \underset{m}{\frac{dV_{GS}}{d\varphi_S}} \underset{n}{\frac{d\varphi_S}{d(log_{10}I_D)}} \tag{1}$$

$$\mathrm{S} = (\ln 10)\frac{dV_G}{d(lnI_D)} = (\ln 10)\frac{dV_G}{d(\beta\psi_s)} = (\ln 10)\left(\frac{kT}{q}\right)\left(\frac{C_{OX}+C_D}{C_{OX}}\right) \tag{2}$$

### *2.4. Some possible ways to decrease SS*

Since the subthreshold current of MOSFET is the minority carrier diffusion current, the relationship between the subthreshold current and $V_{gs}$, i.e., the magnitude of S, will be related to the factors that affect the minority carrier injection efficiency and its movement, as well as the factors that affect the gate control capability. These factors are mainly substrate doping concentration, half-substrate doping concentration, semiconductor surface capacitance, surface conductor surface capacitance, surface state density of states, and temperature. Decreasing the substrate doping concentration and decreasing the semiconductor surface state density, decreasing the depletion layer capacitance and increasing the oxide layer capacitance, as well as decreasing the temperature, can decrease the S value. Thereby, in order to increase the subthreshold operating speed of the MOSFET, the subthreshold operating speed should be minimized when minimizing the interface state interface state and reducing the substrate doping concentration in the gate system of the MOS gate system, and in and reducing the substrate doping concentration, and a certain liner bias voltage should be added when the MOSFET operates (to reduce the depletion layer capacitance) and keep the temperature rise of the device not too large. Bias voltage (to reduce the depletion layer capacitance) and keep the temperature rise of the device not too large. FinFETs can also decrease S factor [6].

### *2.5. Ideal state of SS*

We want the subthreshold swing to be as small as possible; the device is completely off and the source drain current is zero in the subdomain region, i.e., when the gate voltage is less than the threshold voltage. Once the threshold voltage is reached, the transistor turns on rapidly; so ideally the current is very sensitive with respect to voltage changes, i.e. a very small change in gate voltage can cause an order of magnitude change in current. Thus S is small, reflecting better gate control capability and small subthreshold drain current.

Another reason why we need a small subthreshold swing is that the effective subthreshold swing can achieve a large on/off ratio; for example, in a FET, the S factor has a limit of 60mV/decade at room

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temperature, i.e. 300K. The result of this phenomenon is a very large $I_{on}/I_{off}$ ratio, which is really what we want (a ratio as large as possible) because the minimum Ion is used by logic operations or current carrying Capability. A large $I_{on}/I_{off}$ ratio leads to a reduction in static power dissipation in the off-state leakage. To understand this concept, we consider a series of two inverters. One of the inverters will have a higher value in the off state of the MOSFET, and the other will have a lower value because the MOSFET is in the on state. And when the ratio of these two values is greater, the output level will also be better, which can undoubtedly bring about an increase in performance.

A steeper subthreshold slope allows a lower $V_T$ for the same off-current, and it permits the devices to be used at lower supply voltages which attracts the attention for low power operation that has the demand.

### *2.6. Explanation of the limit*

Leakage current exists in MOSFETs and it plays an important role in determining the power consumption of the circuit. Leakage current consists of many components: leakage current through the gate oxide, current through the reverse biased source-drain and drain-drain junctions, Sub-threshold conduction and the decrease in barrier diffusion causes an exponential increase in the density of electrons and increases the leakage current. This is one of the most basic principles of SS limiting. The DOS equation multiplying the DOS equation with the Fermi distribution equation, we obtain a new Eqn (3). This means that electron confusion decreases exponentially with increasing energy. After bringing a temperature of 300 K into the equation, we get 60mV/decade from Eqn (4). In these two equations, $E_C$ is the conduction band edge, $N_C$ is the effective sensitivity of states, $E_F$ is the Fermi energy, $k$ is the Boltzmann constant, and $T$ is temperature in Kevin. This is how we can mathematically prove that the subthreshold swing will have a limit of 60mV/decade [7].

$$n \approx N_C e^{-(E_C - E_F)/kT} \tag{3}$$

$$S(T) \approx ln(10) \cdot \frac{kT}{q} \tag{4}$$

## 3. Tunnelling field-effect transistors(T-FETs)

Moore's law, which was proclaimed in 1975, foresaw the doubling of transistors number in integrated circuits every two years. Moore's law also has direct impact on the computing [8]. To be more specific, every two years, the switching speed of transistors doubles the same time as transistors per chip. Also, just a year before, Robert H. Dennard formulated the Dennard scaling principle, that is, as the supply voltage ($V_{DD}$) and the circuit delays reduce in proportionate to the geometric shrink of transistors while the power consumption stays constant. The development of integrated circuit follows these two laws for nearly 40 years, but the doubling of the switching speed and the Dennard scaling principle all came to the end due to the power consumption problem. Figure 1 shows Dennard scaling and Moore's law. Figure 1 shows that although Moore's law still works, the power consumption of transistors can't be decreased any more. The high switching speed takes enormous energy and at the same time, the reducing of supply voltage can't keep in the same pace of the shrinking of transistors as the aggressive down-scaling of MOSFETs, both of which bring out serious power consumption and heat dissipation.

Driven by the ardor to reduce power consumption and optimize the performance of transistors, various structure and materials of Field effect transistors have been indiscriminately fabricated, such as NC-FETs, II-FETs, FINFETs, Piezo-FETs and TFETs. Among them, TFETs are regarded as the best replacement due to its capacity to overcome sub-threshold slope degradation and offer prominent power consumption savings. Therefore, this chapter will introduce the TFETs' development, principles and performance optimization.

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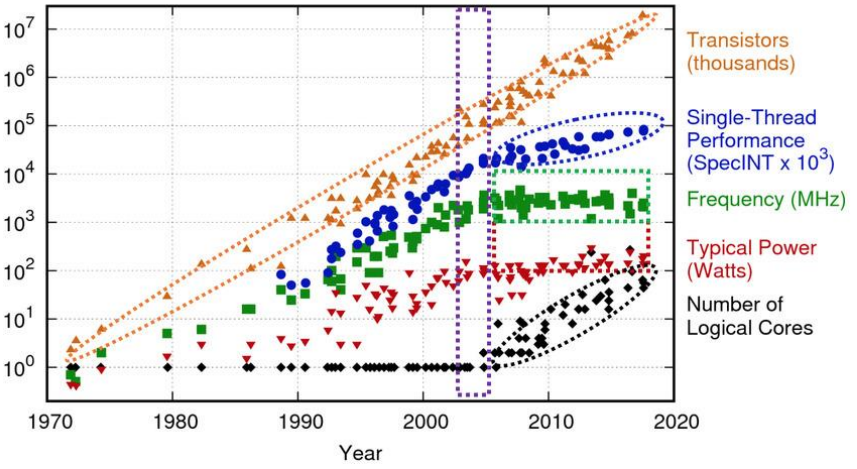


**Figure 1.** Dennard scaling and Moore's law [9].

*3.1. The development of TFETs*

In 1957, the Japanese scholar Esaki invented the Esaki diode, that is, the Tunnel diode [10]. The advent opens a new field of semiconductor devices for which he was awarded the Nobel Prize in Physics in 1973. In 1978, Quinn et al. from Brown University and his collaborators proposed the structure of the TFET device which is a P-I-N diode controlled by the gate voltage [11]. And they speculated that the TFET device may have great development prospects in spectroscopy through experimental studies. After Quinn et al. proposed the TFET structure, Banerjee et al. studied a new three-terminal-controlled TFET device based on Quinn's research [12]. Particularly, Takeda et al. explored the various relevant studies of scaling down [13]. In 1992, Baba et al. fabricated a new three-terminal-controlled tunnelling device called surface tunnel transistor (STT) using III-V compound materials and confirmed the working principle of STT by demonstrating transistor characteristics under the 77k and room temperature [14]. In 1995, Reddick and Amaratunga from the University of Cambridge conducted a large number of experimental studies on the characteristics of silicon-based planar tunnelling transistors [15]. They found that the characteristics of tunnelling transistors were better than that of MOSFETs when the device size was reduced and would not occurs source and drain penetration like a MOSFET. In 2000, Hansch et al.[16] also studied the silicon-based tunnelling transistor. They fabricated the first vertical silicon-based tunnelling transistor in reverse bias, and formed a heavily doped structure by molecular epitaxy [16]. It helps the development of Ultra Large-Scale Integration (ULSI) for its advantages of metal oxide gate dielectric, low supply voltage and exponentially increasing current. In 2004, Aydin and Zaslavsky et al. fabricated the first SOI-substrate tunnelling transistor so that they could reduce the capacitance of the gate and increase the speed [17]. The key difference from other tunnelling transistors is that there is no intrinsic region in this transistor and this tunnelling transistor is a heavily doped gated PN diode.

Researchers have consistently optimized the TFETs after various change of structure and material. It is theoretically believed that TFETs were able to achieve lower Sub-threshold Swing than MOSFET. But this idea has never been realized until Appenzeller invented the Carbon Nanotube Field Effect Transistors (CNFETs) and realized Sub-threshold swing of 40 mv/decade [18]. And this is also the first time human ever realize the Sub-threshold swing lower than 60 mV/decade. After that, Zhang testified that TFETs devices can break through the limitation due to its different work principle --- tunnelling effect in 2006 [19]. In 2007, Woo Young Choi and Byung-Gook Park fabricated the first silicon-based TFETs devices which reached Sub-threshold Swing lower than 60 mV/decade. However, people still find that TFETs own relatively low ratio of on-current and off-current compared to classic MOSFET.

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### *3.2. The principles of TFETs*

In the classical MOSFETs structure which has been demonstrated before, their source and drain region shares the same type of doping and carriers will be able to cross the barrier and pass through the channel while applying sufficient gate bias. Compare to these, TFET devices are generally P-I-N diode structures as shown in Figure 2. Observing the structure, the channel is the I region, which is generally lightly doped or intrinsic state, so the channel region is in a high resistance state and have small number of carriers. Take N-TFETs (Negative TFETs) as an example, the source region is heavily P-type doped and the drain region is heavily N-type doped. The P-TFETs (Positive TFETs) structure is opposite. When applying a positive voltage on the drain area, the TFETs will always be in the reversed-biased. Owing to the large potential barrier in the intrinsic area, it is difficult for the carriers from the source area to enter the drain area through the channel, so the off-state current of the device is very small; when apply positive gate bias, the width of the potential barrier becomes thinner, the source region carriers can tunnel through the channel to the drain region, and the device enters the open state. The main current of TFETs is generated by the bias current, so the resistance of the device is small when it is forward biased, and the resistance value is large under reverse bias, so that the rectification characteristics of the device can be improved.

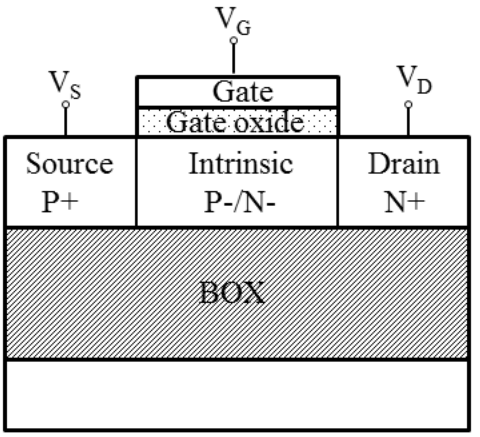


**Figure 2.** The structure of N-TFETs [20].

The prime carrier injection mechanism in the TFETs is band-to-band quantum tunnelling which is called Tunnelling effect. The Tunnelling effect means when a strong electric field occurs at the band bend of the device, electrons may directly go through the potential barrier from the valence band of the semiconductor to the conduction band instead of going through the barrier. In classical theory, a carrier must absorb enough energy larger than the forbidden band width $E_g$ so that the carrier can pass to the conduction band from the valence band. There is no other way to transition from the top to the bottom of the conduction band; and in quantum mechanics theory, a carrier whose energy is not enough to jump over the barrier is not only possible to occur in the barrier region, it is also possible to cross the barrier directly. For N-TFETs, the source region is P-type and the drain region is N-type. When the bottom of the conduction band of drain area is lower than the top of the valence band of the source area, the carries will have tunnelling effect. And a large number of carriers can tunnel from the source to the drain when applying positive bias in the drain area, and the current can flow across devices. This current is on-current and this is the principles of N-TFETs. The principles of P-TFETs is quite similar.

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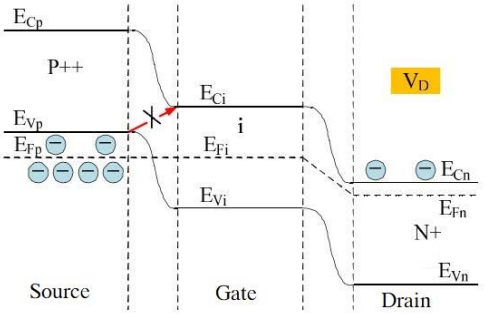


**Figure 3.** Energy Band (Off-state) [2].

TFETs energy band in the off-state is as shown in Figure 3 When the drain of the device is positive biased, the energy band of the drain region is shifted down, and the TFET device is always in a reverse bias state. Meanwhile, the high barrier of the intrinsic region further reducing the off-state current of the device. Therefore, under ideal conditions, the off-state current of a TFET device consists only a small reverse-biased current.

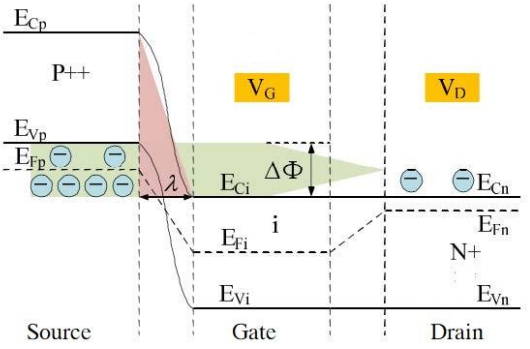


**Figure 4.** Energy Band (Off-state) [2].

Figure 4 shows the energy band of TFETs in the on-state. In the on-state condition, the P-type source of the device is connected to zero voltage, and a positive voltage is still applied to the drain to make the TFET in a reverse-biased state, and the drain voltage is still positive. This voltage needs to make the conduction band bottom of the channel region lower than the top of the valence band of the source region, so that band-to-band tunnelling occurs between the source region and the channel, resulting in the working current of the TFET. However, only those carriers located in the energy window (ΔΦ) own the opportunity to tunnel into the channel while most of the carriers of the source is cut off based on the Fermi distribution resulted in low on-current of TFETs.

### *3.3. Performance optimization*

TFETs own many problems. The source-drain asymmetric doping structure in TFET devices causes a serious bipolar effect, which leads to excessive external power consumption issues. The so-called bipolar effect is that when the gate voltage of the TFET is in a reverse biased state, the load carriers can tunnel through the drain and intrinsic area of the TFET device depending on the tunnelling effect method, and finally flow into the source region to form a reverse tunnelling current. In certain cases, the reverse tunnelling current can be of the same order of magnitude as the forward conduction current. This bipolar conduction effect will bring serious power loss to the actual circuit, so a special design is needed to suppress the bipolar effect in the device design process [21].

Based on the above discussion, we can conclude that for the structure and equipment optimization design of a thousand TFET device, the main consideration should be how to increase the on-current, reduce the leakage current, and improve the sub-threshold swing at the same time. TFET, as a device based on band-to-band tunnelling, transports carriers located in tunnel junction between the source and

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the intrinsic area. Therefore, the probability of tunnelling determines the tunnelling current of the TFET device.

The band-to-band-tunnel (BTBT) transmission probability ($T_{WKB}$) can be calculated using Wentzel-Kramer-Brillouin (WKB) approximation [22, 23]:

$$T_{WKB} \sim exp\left(-\frac{4\lambda\sqrt{2m^*E_g^3}}{3qh\left(E_g+\Delta\varphi\right)}\right) \tag{5}$$

Among Eqn (5), $m^*$ is the effective carrier mass and $\lambda$ is the tunnelling distance. As mentioned above, the drain voltage of the TFETs keeps constant, when the gate bias increase, tunnelling distance $\lambda$ will be reduced and set apart the conduction band of the source and the valance band of the drain, which means the increasement of $\Delta\Phi$. According to Eqn (5), $T_{WKB}$ can be maximized by minimizing $\lambda$, $m^*$, $E_g$ on the propose of achieving a adequate on-current. In reality, $m^*$ and $E_g$ solely rely on the material system and both material system and device structure can deeply affect $\lambda$. In conclude, the performance optimization of TFETs should mainly focus on selecting an appropriate material system and set the best device geometry. In the next chapter, we will introduce how the material of TFETs can overcome sub-threshold slope degradation.

## 4. Materials of TFETs

### *4.1. SS in TFETs*

In order to overcome the sub-threshold slope degradation, we can change the materials of TFETs. According the definition of SS and the formulas of TFET mentioned above, the expression of SS in TFET can be deduced as Eqn (6) [24].

$$SS = \ln(10)\left[\frac{1}{V_{eff}}\frac{dV_{eff}}{dV_G}+\frac{\xi+b}{\xi^2}\frac{d\xi}{dV_G}\right]^{-1} \tag{6}$$

The first item in the formula relates to structure and the second item to material, where $b$ is a parameter related to $E$, the band-gap width:

$$b = \frac{4\sqrt{2m^*}E_G^{3/2}}{3q\eta} \tag{7}$$

Some materials have smaller band-gap width. From the Eqn (7), if E becomes smaller, b becomes smaller. Then the SS becomes small.

In addition, the band-gap width can also influence the on-state current I as the Eqn (8) shown:

$$I = aV_{eff}\exp\left(-\frac{b}{\xi}\right) \tag{8}$$

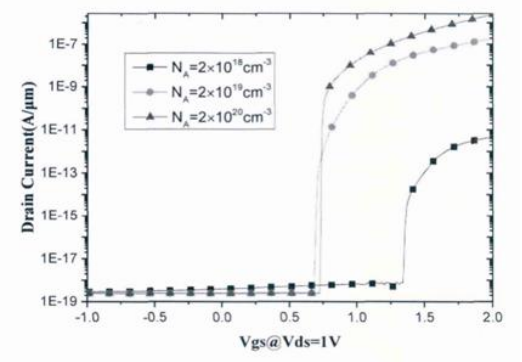


**Figure 5.** Diagram of the relationship between on-state current and subthreshold slope [24].

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If *E* becomes smaller, the on-state current *I* will becomes larger. And as the figure 5 showing, if the on-state current turn larger than the subthreshold slope becomes sharper.

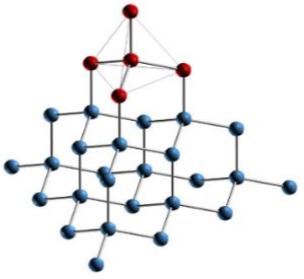
### *4.2. Some research popular materials*

Low power integrated circuits require that TFET devices should not only have ultra-steep subthreshold swing, but also have low off current and high on current. Although in theory, TFET devices can obtain sub threshold swing lower than 60mV / decade at room temperature and have low off state current, it is still difficult to obtain ultra-steep sub threshold swing in the actually prepared devices, and TFET devices face problems such as low on state current and bipolar characteristics, so it is still difficult to be widely used in practical circuits at present [25]. Therefore, how to obtain a higher on-state current while ensuring a lower off-state current in TFET devices, and maintain an ultra-low subthreshold swing in a large current range is an urgent problem to be solved in the current TFET research, and these problems urge researchers to continue to conduct in-depth research. This part will give some research popular materials including group IV materials, III-V materials, and some other new ones [26].

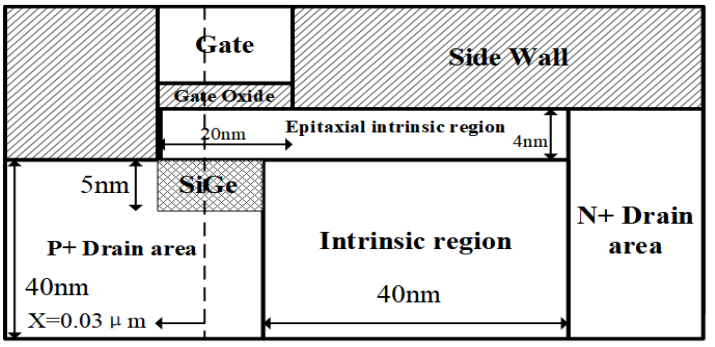
### *4.3. Group IV materials*

In traditional group IV materials, the open-state current is relatively low in both simulation and experimental results. However, TFET devices based on Si(silicon) and Ge materials have very good low threshold retention characteristics and can be compatible with the CMOS processes. It is very promising to be applied at the earliest time, so it still has great research value. At present, the more common research is using Si/Si1-xGex heterojunction.

The lattice structure of both Si and Ge is diamond structure (Figure 6 (a)), which can be melted to form alloy materials in any proportion. To apply this material in the intrinsic zone, can effectively reduce the band gap width and facilitate the tunnelling of carriers. In TFET devices, the SiGe band gap of low Ge components are similar to that of Si. In addition, strain technology often uses SiGe as a virtual substrate to grow strain channels on this layer, which improves the mobility of device carriers, thereby increasing the drive current of the device and suppressing some short channel effects. In order to discuss the effect of SiGe/Si Heterojunction on tunnel, SiGe material is used in the source region of TFET devices. P-type impurity doping is used to form SiGe/SiGe heterojunction between the source region and the extended eigen region (Figure 6 (b)). When the doping concentration of both components is the same, the SiGe band will increase relative to the Si band [24]. When the SiGe layer is in contact with the Si layer in the intrinsic region, the tunnelling distance of the carrier decreases. Due to the smaller bandwidth of this material, it can effectively increase the tunnelling probability of the carrier and reduce



(a)




(b)

**Figure 6.** (a) shows the structure of both Si and Ge, (b) shows a kind of SiGe TFETs[24].

SS.

Figure 6 shows the structure and electrical characteristics of U-type TFET based on the SiGe materials compared to the traditional one.

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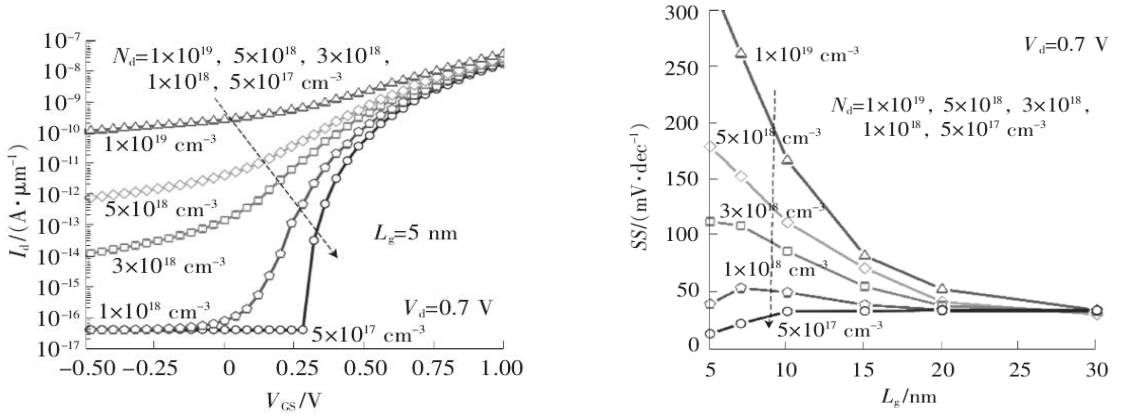
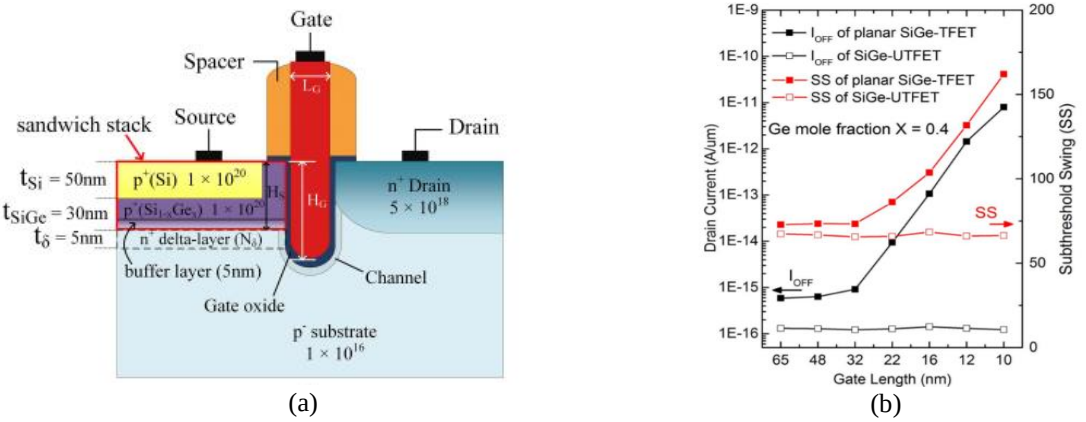



(a) (b)

**Figure 7.** (a) shows the $I_D$–$V_{GS}$ Curve of Device at $L_g$=5nm, (b) shows the Effect of SS and Nd on Different Gate Length Devices [25].

In Figure 7, it shows the influence of TFET drain doping concentration (nd) on devices with different gate lengths in TFET devices based on silicon materials. The study found that the lower the drain doping concentration, the smaller the off-state current, but has little effect on the on-state current of the device. With the reduction of the gate length of the device, the influence of drain doping concentration on the subthreshold swing becomes larger.




(a) (b)

**Figure 8.** (a) the device structure, (b) dependence of IOFF and SS of planar TFET and UTFET on-gate lengths 0.

According to the previous analysis, the introduction of SiGe material into Si-based materials can adjust the band gap width at the tunnel junction and improve the chances of tunnelling of the carrier, but the increase of tunnelling current is still limited, and the TFET device is still low on-state. If the Ge component is continuously improved, a series of reliability problems will occur and strain relaxation will occur inside the TFET device [24]. The introduction of Ge component in the channel region will make the Ge atom diffuse, increase the carrier scattering process during transport, reduce the carrier drift speed, and decrease the device drive current. In addition, the thermal conductivity of Ge material is less than that of Si material, and the heat energy generated by the current of the device is harder to emit, which causes the autothermal effect inside the TFET device and affects the normal use of the device.

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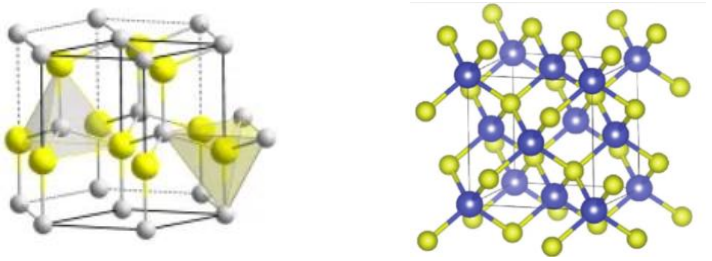
### *4.4. Group III-V Materials*

Due to the high mobility, direct band gap, narrow band gap and lower quality of carrier tunnelling, the III-V materials are very advantageous to improve the channelling probability of carriers and obtain higher on-state current [28]. It has been found that when channel material is changed from Si to InAs or InSb in TFET devices, the current increases by several orders of magnitude. At the same time, the use of heterostructures can further reduce the tunnelling distance to obtain higher open-state current and ultra-steep sub-threshold swing [26].



(a) (b)

**Figure 9.** (a) wurtzite structure, (b) sphalerite structure[24].

The lattice structure of III-V compound semiconductor materials is usually wurtzite structure or sphalerite structure (Figure 9). These structures are mainly composed of two different types of atoms. They have no central symmetry and have piezoelectric polarization effect [27]. Under the applied stress, the crystal lattice will be distorted, resulting in the separation of positive and negative charges, forming a dipole moment. When the dipole moment accumulates to a certain extent, the polarized charge will appear on the crystal surface, showing the piezoelectric polarization effect. In addition, the crystalline symmetry of the wurtzite structure is lower than that of the sphalerite structure, and the positive and negative charge centers are separated even when there is no stress, so the spontaneous polarization effect occurs along the polar axis [24]. In this way, when a thin III-V layer is used in TFET devices, a large polarization electric field can be formed by using the potential difference caused by the polarization charges on both sides of III-V. When the direction of this field is consistent with that of the grid electric field, the internal electric field of the device can be increased. Therefore, it can improve the performance of TFET devices and reduce SS.

Many researchers have made lots of efforts in this field. Some examples show in Figure 10, which compares the SS of these TFETs [25].

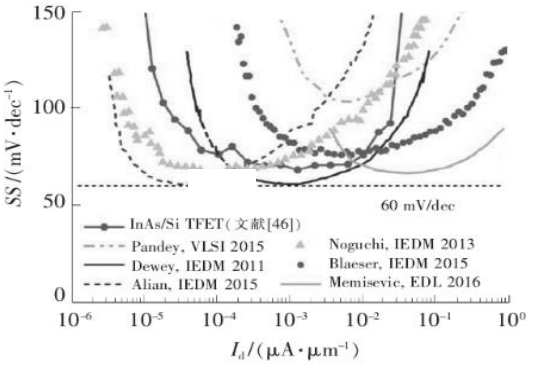



**Figure 10.** Experimental results of TFET devices [25].

### *4.5. Other materials*

In recent years, TFET devices based on GeSn materials have attracted much interest from researchers. Group III-V materials are not suitable for preparing P-type TFETs because of their low electronic

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density of states [25]. Complementary TFETs (CTFETs) cannot be achieved and are compatible with Si substrates. As group IV materials, TFET devices based on GeSn materials have been extensively studied and have achieved high device performance because of the transition to direct band gap materials by increasing the Sn content in the materials, which leads to direct tunnelling [26]. GeSn materials have narrower band gaps than traditional group IV materials, and can change from indirect band gaps to direct band gaps by adjusting the composition rate of materials. GeSn materials have the characteristics of easier integration with Si substrates than group III-V materials. Based on these characteristics, a large number of studies have found that this kind of TFET has a higher tunnelling probability, which can lead to higher on-state current and lower SS.

## 5. Conclusion

This review showed the necessity to overcome Sub-threshold slope degradation, and showed how the advances of TFETs Material can significantly lower SS. Transistors scaling has always under the push of Moore's law for the last half century. But, this scaling behavior arises a lot of problem such as short channel effect and increasement of power consumption, which is a main challenge in IC industry. Most of the power consumption comes from switching power consumption, which comes from the switching of devices. Sub-threshold Slope act as an essential factor using to reflect this change. In classical MOSFET devices, Sub-threshold Slope can only be minimized to 60 mV/decade due to "Boltzmann Tyranny". TFETs are promising candidates to MOSFET owing to their potential to overcome this limitation. This article introduces the principles of TFETs --- tunnelling effect. By illustrating these, we can conclude that choosing an approving material system and set the best devices architecture are the main ways to optimize TFETs performance. Researchers have done lots of works in such fields including group IV materials, III-V materials. In recent years, TFET devices based on GeSn materials have attracted much interest from researchers.

In spite of the hard work mentioned above devoted into choose the best material system to overcome Sub-threshold slope degradation, Scientists have explored other method including change of TFETs structure and other field-effect transistors. The former method consists of various categories of line tunnelling types TFETs, involving L-shaped TFETs (LTFETs), Z-shaped TFETs (ZTFETs) and U-shaped TFETs (UTFETs) [31]. Among them, LTFETs are the most deserving studied because they are the only to be experimentally demonstrated. As for other field-effect transistors, there are negative capacitance field-effect transistors (NC-FETs), impact ionization field-effect transistors (II-FETs) and cold source field-effect transistors (CS-FETs) [34]. All of them are both energy efficient and ignoring "Boltzmann Tyranny". But, although remarkable progress and significant efforts have been made, overcoming Sub-threshold Slope degradation still has a long way to go.

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