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Silicon Sunk Costs: The Semiconductor Industry's Reliance on Obsolete Technologies

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Abstract: Moore's Law has long driven the semiconductor industry's pursuit of miniaturization, yet firms continue investing in mature nodes (e.g., 28nm/200mm fabs) due to the powerful sunk cost fallacy. This phenomenon distorts rational decision-making, trapping companies in outdated technologies despite the availability of more advanced alternatives. This paper develops a framework that integrates technical rigidity, behavioural commitment, and institutional lock-in to explain this paradox, challenging conventional market-demand narratives. By introducing the Sunk Cost Escalation Multiplier (SCEM), this research identifies critical thresholds where continued investment transitions from strategic to irrational. The analysis highlights how industry structure and cognitive biases interact to sustain technological lock-in, presenting significant policy implications for capital reallocation and technology transition roadmaps. It further illustrates how sunk costs create self-reinforcing cycles: specialized equipment with long lifespans, such as 200mm fabs, becomes economically obsolete yet remains physically operational. Additionally, policy incentives like subsidies often inadvertently perpetuate these inefficiencies, hindering innovation and progress.

Keywords: Sunk cost fallacy, semiconductor, decision-making, technological obsolescence

1. Introduction

The semiconductor industry's relentless pursuit of Moore's Law has long driven successive waves of miniaturization [1]. Paradoxically, firms continue to expand legacy production lines—such as 28nm processes on 200mm wafers—despite the superior cost performance of advanced nodes. In 2023, global semiconductor R&D spending reached approximately $98.8 billion [2]. Yet, the 200mm fab capacity is projected to increase by 14% from 2023 through 2026, with 13 new 200mm volume fabs expected to be added during this period, indicating a significant persistence of outdated assets [3].

This persistence reflects a sunk cost trap, where prior investments irrationally influence decision-making. Drawing on Thaler's behavioural economics and Arkes and Blumer's experimental evidence, this research contends that semiconductor firms, like consumers, faces escalation of commitment, resulting in inefficient resource allocation [4-5]. To evaluate this inefficiency, this research proposes the Sunk Cost Escalation Multiplier (SCEM), a novel metric to quantify when further investment in mature technologies becomes economically irrational. Although 200mm fabs face mounting challenges—such as dependence on scarce second-hand equipment with lead times of 18–24 months and maintenance costs comprising up to 30% of total operating expenses—firms

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continue to expand them, suggesting entrenched irrationality [6]. A tripartite framework is proposed to explain this inertia: technical rigidity, behavioural bias, and institutional lock-in.

By unpacking these interdependent mechanisms, this study explores how sunk cost traps manifest in semiconductors and the role of technical, behavioural, and institutional rigidities. This paper focuses on why firms continue to invest in legacy nodes despite the economic superiority of advanced nodes. Rather than reflecting market rationality, continued support for mature nodes often stems from behavioural bias and institutional inertia. Recognising this misalignment is key to designing policies and strategies that promote more efficient, forward-looking capital allocation.

2. Quantitative evidence: the Sunk Cost Escalation Multiplier (SCEM)

2.1. GlobalFoundries' mature node strategy in industry context

GlobalFoundries (GF), the world's third-largest pure-play foundry, specializes in mature process nodes (28nm and above) and differentiated technologies, including its 22FDX+ platform [7]. The company primarily serves the automotive, IoT, and 5G sectors. In 2023, GF invested $4 billion to expand its 300mm wafer fabrication facility in Singapore, aiming to increase annual capacity by 450,000 wafers, thereby bringing the total to approximately 1.5 million wafers per year. Its Singapore plant, which already serves more than 200 customers globally, is projected to contribute approximately 30 percent of the company's revenue in 2024 [8]. However, but earnings reports show that margins in its mature process business are below the industry average [9].

UMC, the world's fourth-largest foundry, reported a capacity utilization rate of only 70% in Q4 2024, with its 200mm lines operating at around 50%, reflecting weak demand for mature nodes. Rumors of a merger between UMC and GF indicate a consolidation of mature node capacities to better compete with Chinese foundries [10]. However, even post-merger, their combined market share would be around 9%, still trailing behind TSMC (67%) and Samsung (8.1%) [9].

2.2. Sunk Cost Trap Multiplier (SCTM) analysis

This paper uses 2 tables to analyze the Sunk Cost Trap Multiplier. Table 1 shows the cost comparison between 200mm and 300mm fabs.

Table 1: 200mm and 300mm fabs [10-14]

Cost Component	200mm Fab	300mm Fab
Equipment Investment	Relies on second-hand equipment; prices vary widely ($5-10M per photolithography equipment)	Standardized new equipment; price of a used 200mm core is more expensive than an equivalent 300mm core.
Wafer Utilization	Approximately 31,400 mm² (0.0314 m²) (fewer chips)	Approximately 70,685 mm² (0.0707 m²) (2.25x more chips)
Unit Chip Cost	High ($1.61 per chip)	Low ($1.14 per chip; 29% cost reduction)
Maintenance Costs	30% of total operating expenses (complex maintenance for aging equipment)	15% of total operating expensesl; High level of automation and standardisation of equipment have a relatively low percentage of maintenance costs.

Table 2 indicates the difference of unit chip cost between 200mm fab and 300mm fab.

Table 2: Unit chip cost

	200mm Fab	300mm Fab
Equipment Investment	$1.5B (premium for second-hand equipment)	$400 billion (standardized new equipment)
5-Year Total Cost	$5.4B (including manufacturing and maintenance)	$8.52 billion
Unit Chip Cost	$0.29 per chip	$0.20 per chip (31% lower cost)

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Table 2 illustrates that 300mm fabs offer significantly lower unit chip costs compared to 200mm fabs, with economies of scale offsetting higher initial investments.

2.3. Manifestations of the sunk cost trap in the industry

The semiconductor industry faces significant equipment lock-in challenges, particularly since 200mm wafer tools cannot be retrofitted for 300mm production, forcing firms to maintain obsolete production lines. For instance, UMC's 8-inch fabs operated at just 50% capacity in 2024, yet the company still incurred depreciation and maintenance costs for underutilized equipment—a clear demonstration of sunk costs' persistent drag [9]. This misallocation of resources not only restricts firms' ability to transition to advanced nodes but also creates substantial opportunity costs, as capital remains tied up in inefficient assets rather than being deployed for technological upgrades [9].

While short-term demand for mature-node chips remains stable in sectors like automotive and industrial, their long-term growth (~5% CAGR) lags far behind advanced nodes (e.g., AI chips at ~20% CAGR) [9]. Compounding this pressure, China is rapidly expanding mature-node capacity and is projected to account for 50% of global additions within 3-5 years, further eroding the market share of incumbents like UMC and GF [10]. This structural market shift leaves legacy-node-dependent manufacturers stranded: persisting with existing capacity risks losses from demand attrition, while pivoting to advanced nodes requires prohibitively high investments.

2.4. Industry trends and policy impacts

The semiconductor industry faces intensifying pressure to adopt advanced technologies, as exemplified by TSMC's aggressive investment of over $100 billion in 3nm and 2nm fabs in the U.S., which is eroding profit margins for mature-node production [9]. While some firms attempt differentiation strategies—such as GlobalFoundries' 22FDX+ platform targeting IoT and 5G niches—these specialized processes address limited markets and fail to support long-term growth, leaving companies vulnerable to technological displacement [7].

Policy interventions further skew the competitive landscape. The U.S. CHIPS Act prioritizes subsidies for advanced-node R&D, inadvertently marginalizing mature-node investments (e.g., by restricting China's equipment access). In response, firms like GF and UMC are exploring mergers to consolidate mature-node capacities, but their shared lack of sub-12nm capabilities exposes a critical technological gap, limiting their ability to compete with industry leaders [10].

2.5. Conclusions and recommendations

The persistence of 200mm wafer production exemplifies economic irrationality, as 300mm fabs demonstrate 29-31% lower per-unit chip costs and superior long-term ROI. However, expanding 200mm capacity relies on a precarious second-hand equipment market with 18-24 month lead times, while maintenance consumes up to 30% of operating expenses - creating a vicious cycle of diminishing returns [9]. To escape this sunk cost trap, firms must strategically transition to 300mm or advanced packaging solutions like chiplets, while preserving only specialized process lines (e.g., automotive MCUs) and halting new investments in obsolete technologies. This shift carries broad industry implications, particularly for Chinese manufacturers like SMIC that risk overcapacity in mature nodes (e.g., 28nm expansion) amid shrinking global demand.

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3. Tripartite lock-in framework

3.1. Technical rigidity

Technical rigidity can be defined as a company's inability or reluctance to adopt new technologies due to the high cost or complexities related to upgrading existing systems. Advances in technology have given rise to the integration of novel processes into legacy systems. However, the financial implication can prove prohibitive, resulting in firms continuing to utilise outdated technologies.

The increasing costs of EUV lithography tools are indicative of a technical rigidity in semiconductor manufacturing. ASML's Low-NA EUV systems are priced at approximately $183 million, whereas the next generation of High-NA Twinscan EXE machines are expected to cost around $380 million each [15]. The substantial expenses incurred in the retrofitting of legacy fabs with EUV technology serve to reinforce a reliance on existing processes, thereby hindering technological advancement. Similarly, Intel's delayed transition to 10nm technology serves to illustrate the consequences of overly ambitious planning. The 10nm process was initially scheduled for 2016 but was delayed due to yield issues and aggressive design goal [16]. This misstep disrupted Intel's product roadmap and allowed competitors to gain market share.

3.2. Behavioural bias

Behavioural bias in organisations is defined as the tendency of decision-makers to favour familiar technologies or processes, even when newer alternatives may offer superior performance or efficiency. Cognitive biases, such as status quo bias, have been shown to influence managers' preferences, resulting in a preference for existing technologies [17]. This bias can impede innovation and adaptation to new advancements.

For instance, in 2022, NXP disclosed a procurement commitment to its foundries amounting to $4 billion, primarily for capacity expansion of mature process nodes. This decision is indicative of a preference for established technologies over newer, potentially more efficient alternatives. Furthermore, Texas Instruments reported its revenue for the fourth quarter of 2021 increased by 19% in comparison with the same quarter a year ago [18]. This growth signifies a persistent reliance on established process technologies, despite the existence of more recent alternatives.

3.3. Institutional lock-in

Institutional lock-in occurs when external policies or incentives act as a disincentive to the implementation of technological upgrades [19].

China's 28nm semiconductor subsidy program is a case in point. The programme was initiated as part of the "Made in China 2025" initiative, with the objective of offering substantial tax incentives to firms utilising 28nm or larger process nodes. Specifically, projects operating for over 15 years are eligible for up to 10 years of corporate income tax exemption, while those using 65nm to 28nm processes receive five years of tax exemption followed by a 50% discount for the next five years [20]. These policies have been shown to have a significant impact on the financial incentives of firms, discouraging the adoption of newer technologies and thereby perpetuating the use of older process nodes. This has the potential to stifle innovatio n. For instance, in 2022, China allocated over $1.75 billion in subsidies to 190 semiconductor firms, with the largest recipient, Semiconductor Manufacturing International Corporation (SMIC), receiving $282.1 million [21].

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4. Escaping the trap: comparative case studies

The Tripartite Lock-in Framework provides a theoretical model that illustrates how firms become entrenched in existing technologies because of interdependent forces. The following case studies of TSMC's CoWoS and Intel's Embedded Multi-die Interconnect Bridge (EMIB) provide practical examples of how companies navigate and potentially escape such technological entrapments.

The utilisation of a silicon interposer facilitates the connection of multiple chips, thereby offering high interconnect density and bandwidth. This feature is paramount for AI and high-performance computing applications. TSMC has announced its intention to double its CoWoS capacity by 2025 in order to meet the increasing demand for artificial intelligence [22]. The technology utilises a silicon bridge embedded in the substrate for the purpose of interconnecting chips, thereby providing a cost-effective solution with high interconnect density. EMIB has been successfully implemented in Intel's Stratix 10 and Kaby Lake-G products, thereby demonstrating its scalability and performance [23].

The Resource-Based View (RBV) states that firms gain competitive advantage through unique resources and capabilities. TSMC's expertise in silicon manufacturing supports its CoWoS strategy, while Intel's EMIB utilises its strengths in substrate engineering. This divergence reflects each company's strategic alignment with its core competencies [24].

5. Policy recommendations

To enhance Europe's semiconductor resilience, it is essential that policy support adheres to the principle of technology neutrality, as outlined in the EU Chips Act Article 17 [25]. This ensures that subsidies and incentives are based on market demand and strategic importance, rather than favoring specific technologies. For instance, while advanced nodes like 5nm are crucial for AI and high-performance computing, mature nodes such as 28nm remain vital for automotive and industrial applications, constituting approximately 75% - 80% of global foundry capacity [26].

By embracing technology neutrality, the EU can foster a balanced semiconductor ecosystem that supports both cutting-edge and foundational technologies. This strategy has been demonstrated to enhance industrial resilience and aligns with global best practices, thereby ensuring that Europe's semiconductor policies are inclusive and forward-looking.

6. Conclusion

The present study reveals that the persistence of mature semiconductor nodes (e.g., 28nm/200mm fabs) stems not from market rationality but from a tripartite sunk cost trap: technical rigidity (EUV incompatibility, retrofitting costs), behavioural bias (status quo preferences), and institutional lock-in (misaligned subsidies). The Sunk Cost Escalation Multiplier (SCEM) framework is a tool used to analyse the economic implications of decisions made regarding the adoption of legacy technologies. It has been demonstrated that decisions to expand capacity through suboptimal means, as exemplified by the capacity expansions undertaken by GlobalFoundries and UMC, can result in economically irrational outcomes when firms fail to transition to more efficient alternatives. In order to combat these inefficiencies, it is incumbent upon policymakers to prioritise technology-neutral incentives and residual value thresholds, with a view to aligning capital allocation with technological frontiers.

However, this study may benefit from a more detailed empirical analysis of specific case studies to better illustrate the mechanisms of the sunk cost trap in different market contexts.

Looking ahead, future research can explore the manner in which emerging innovations, such as advanced packaging, disrupt the aforementioned traps, thus offering pathways to reconcile Moore's Law with sustainable industrial upgrading.

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