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Research on the reliability of gate oxides in SiC MOSFETs

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Abstract. SiC MOSFETs are highly regarded in modern electronic devices due to their exceptional high-temperature performance, high power handling capability, and high-frequency operation. Nevertheless, the reliability of these devices, particularly concerning the stability of the GOX layer and the density of boundary state, poses significant limitations to their potential applications in extreme environments. This paper provides a systematic study of the reliability challenges encountered by SiC MOSFETs in practical applications, emphasizing the effects of gate oxide layer stability and interface state density on device performance. The findings indicate that interface defects and epitaxial layer quality are the primary determinants of gate oxide layer reliability. Additionally, this paper explores various reinforcement strategies to mitigate these issues.

Keywords: SiC MOSFETs, gate oxide, reliability, reinforcement methods.

1. Introduction

With the advancement of modern electronic technology, the demand for high-power, high-efficiency electronic devices is escalating. Silicon carbide (SiC) is deemed an ideal material for the next generation of high-power electronic devices due to its outstanding material characteristics, including a Extensive energy bandgap, outstanding heat conductivity, and high electric field strength [1-3]. Compared to traditional silicon-based devices, SiC MOS devices demonstrate higher reliability and efficiency under extreme conditions such as high thermal levels, high-frequency, and high power intensity. This superiority is attributed to SiC's wider bandgap , which facilitates a low intrinsic charge density even at elevated temperatures [1-3]. Furthermore, the high thermal conductivity of SiC enhances heat dissipation efficiency, thereby improving device stability and lifespan [1]. The high breakdown electric field of SiC permits operation at higher voltages without significant risk of breakdown. These advantages render SiC MOSFETs particularly suitable for applications such as electric vehicles, where their high efficiency and reliability are crucial for inverters and charging systems [1,3].

The GOX of SiC MOSFETs is a critical component, with its reliability directly impacting the performance and lifespan of the device. Despite the traditional thermal oxidation process forming an oxide layer on SiC, issues such as interface defects and near-interface traps (NITs) persist, leading to low channel mobility and suboptimal oxide reliability [4]. To enhance MOSFET performance, researchers have extensively explored post-oxidation annealing (POA) treatments, including annealing in nitrous oxide (NOx) or nitric oxide (NO) atmospheres, to improve interface characteristics and oxide quality [2]. These studies have focused on the breakdown mechanism and TDDB behavior of the GOX.

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Breakdown electric field (EBD) and breakdown charge (QBD) are two critical parameters for assessing gate oxide reliability [4,5]. Xu et al. investigated that the high-heat NO annealing effects the oxide robustness of 4H-SiC MOS capacitors and discovered that high-temperature annealing significantly enhances oxide lifespan and reliability [4]. Research by Wan et al. indicated that controlling the thermal oxidation temperature can significantly reduce the interface state density (Dit) without the need for additional passivation treatments, thereby improving the reliability of the gate oxide.

Moreover, carbon emission-related defects and traps created during the thermal oxidation process are significant factors contributing to early breakdown. Zheng et al.'s research demonstrated that early breakdown is closely associated with large pit defects in the epitaxial layer, which can cause local electric field concentration and accelerate breakdown [5]. Therefore, improving the epitaxial layer's quality and reducing defect density are crucial for enhancing the reliability of SiC MOSFETs.

Recent studies have also examined the impact of nitrogen oxide and hydrogen-nitrogen hybrid passivation treatments on the performance of 4H-SiC MOS devices. Vidarsson et al. found that passivation can significantly reduce the interface state density, though it may introduce fast near-interface traps that limit device electron mobility. Jia et al. proposed a hybrid passivation method combining high-temperature wet oxidation with short-time passivation, incorporating hydrogen and nitrogen atoms to reduce interface states and near-interface traps, thereby enhancing gate oxide reliability and electron mobility.

The outline of this paper is arranged in the following manner: Section 2 delves into the reliability challenges encountered by SiC MOSFETs in real-world applications, particularly emphasizing the effects of gate oxide layer stability and interface state density on device performance. Section 3 explores various methods to enhance the robustness of the GOX layer in SiC MOSFETs. Finally, Section 4 presents the conclusions of the study.

2. Reliability Issues of Gate Oxides in sic MOSFETs

SiC MOSFETs' potential for high-power and high-temperature applications is clear. Nonetheless, their widespread adoption is hindered by significant reliability challenges, particularly concerning the stability of the GOX layer and the density of boundary state. This section provides a detailed discussion of these reliability issues, delving into the specific factors influencing them as identified by recent research. We will examine how these factors impact the performance and longevity of SiC MOSFETs, focusing on the mechanisms behind gate oxide layer instability and the role of interface state density in device degradation. Additionally, we will explore how external conditions such as temperature and electric fields exacerbate these reliability issues, drawing on empirical data and case studies to illustrate the underlying problems and potential solutions.

2.1. Instability Factors of the GOX Layer

The robustness of SiC MOSFETs GOX layer largely influence the SiC MOSFETs' performance and longevity. Studies indicate that at elevated temperatures, the gate oxide layer in SiC MOSFETs possesses an intrinsically long lifespan. Nonetheless, the primary issue is the presence of numerous extrinsic defects, which can lead to premature failure. Hsu et al suggested a theoretical model to account for these initial failures, suggesting that these defects are due to point defects grown in the GOX of SiC MOSFETs rather than traditional theories of local thinning caused by contamination [6].

Under enhanced electric fields, these defects lead to early failure of the oxide layer through an enhanced trap-assisted tunneling current. Additionally, local electric field enhancement remains a significant factor in the extrinsic failure of the GOX layer of SiC MOSFETs, requiring continuous improvement. This local electric field enhancement may originate from deep micro-pits, stacking faults, doping non-uniformities, and non-planar surfaces caused by etching. Figure 1 shows the Weibull distribution graph for SiC MOS TDDB under gate potentials of 42V, 43V, and 44V at a temperature of 175°C [6].

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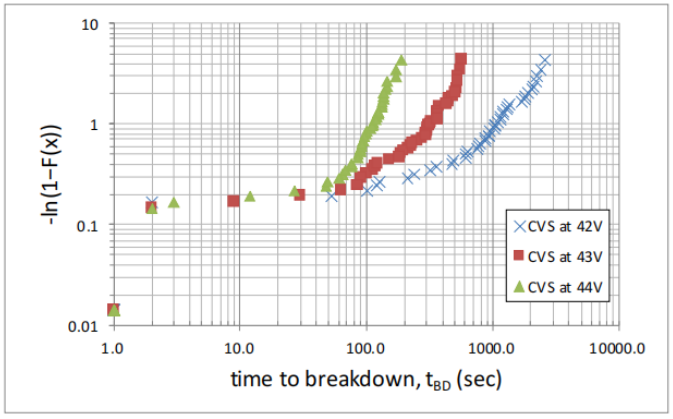

Figure 1. Weibull distribution graph for SiC MOS TDDB under gate potentials of 42V, 43V, and 44V at a temperature of 175℃ [6].

2.2. Impact of Interface State Density on Device Performance

The performance of SiC MOSFETs is significantly influenced by the boundary state Dit). High Dit levels restrict the channel mobility of the device, leading to increase on-resistance and impacting switching characteristics. Research indicates that high-temperature dry oxidation can effectively mitigate interface state density. For instance, Wan et al. demonstrated that SiC MOSFETs oxidized at 1450°C exhibit the lowest Dit, whereas those oxidized at 1250°C show optimal oxide reliability [7].

Moreover, nitrogen oxide (NOx) annealing has proven effective in reducing Dit, albeit potentially causing threshold voltage (Vth) drift. Xu et al. analyzed SiC MOS capacitors under various NOx annealing conditions, highlighting that high-temperature treatments significantly enhance oxide lifespan and reliability. Figure 2 illustrates the Dit profile at ambient temperature, plotting it against the sub-conduction band energy level in SiC, utilizing the C-ψs method. It compares oxidized test samples at temperatures ranging from 1200°C to 1550°C. Similarly, Figure 3 depicts Dit at the SiC interface, correlating with the sub-conduction band energy level in SiC, employing the high-low method and comparing samples oxidized within the same temperature range [4].

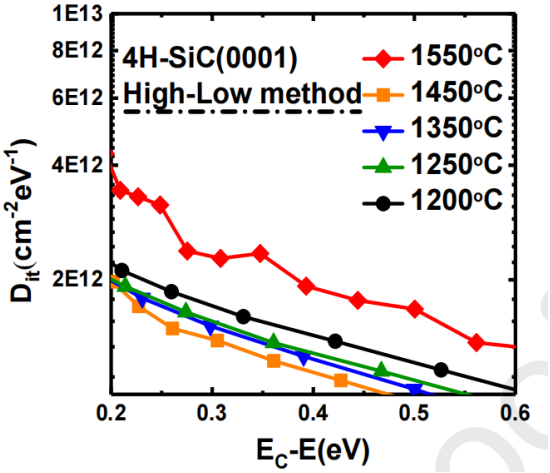

Figure 2. Dit profile for SiO_2/SiC at ambient temperature, calculated using the C-ψs technique. Comparisons are made between five oxidized test samples from 1200℃ to 1550℃. [4].

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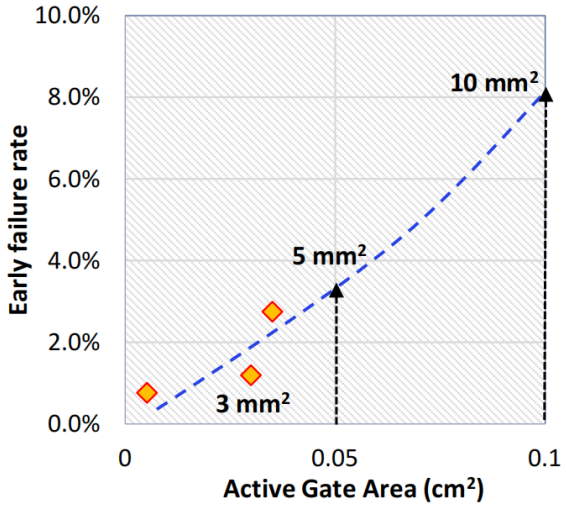

Figure 3. Dit at the SiO_2/SiC interface at 25℃ , determined using the high-low method. The comparison includes five oxidized test samples from 1200℃ to 1550℃ [4].

2.3. Early failure issues

To investigate early failure mechanisms in SiC MOSFETs, researchers have adopted the voltage ramp (vramp) test method. Zheng et al. observed that initial breakdowns associate significantly with prevalence of large pit defects in the epitaxial layer, with a higher gate area leading to increased early failure rates [5].

These early failures predominantly arise from interface traps and oxide defects, which facilitate failure through trap-assisted tunneling mechanisms under high electric fields. Therefore, enhancing the epitaxial layer's quality and optimizing the oxidation process are critical for mitigating early failures. Figure 4 depicts the early life testing results, illustrating the failure rate of gate oxide relative to gate area [5].

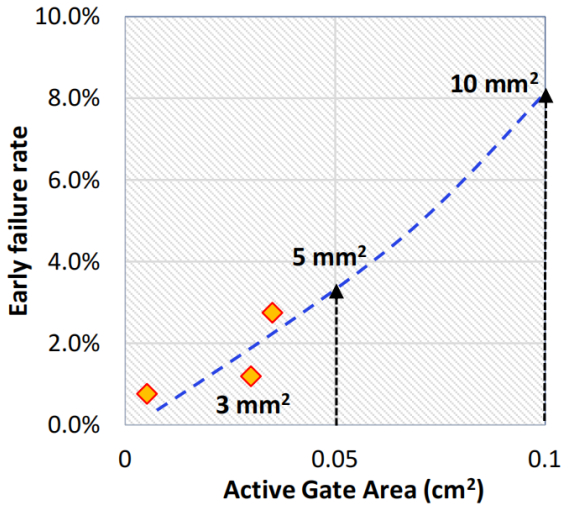

Figure 4. Failure rate of gate oxide as a function of gate area in early life testing [5].

2.4. Thermomechanical stress issues

Ugur et al. underscored the significance of thermomechanical stress on the reliability of SiC MOSFETs [7]. Their research highlighted that high-temperature cycling can degrade the gate oxide, and in certain instances, bond line fractures emerge as the primary cause behind abrupt increases in forward resistance

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and Intrinsic diode voltage. Through de-capsulation analysis of failed devices, researchers were able to pinpoint early indicators of degradation and evaluate the prolonged dependability implications of thermomechanical stress on SiC MOSFETs. Figure 5 illustrates the transfer characteristics for 2C-5 samples over multiple power cycles [7].

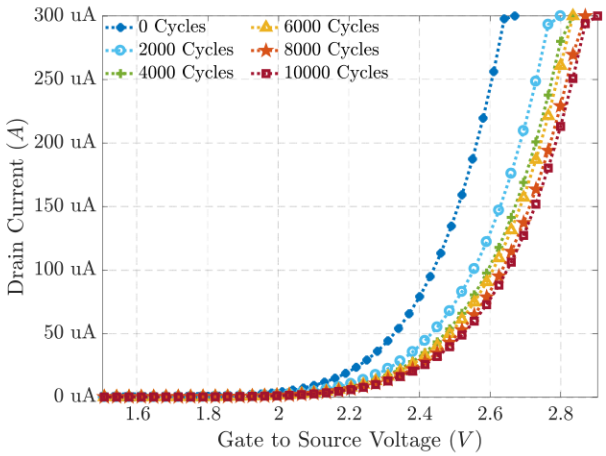

Figure 5. Transfer characteristics for 2C-5 samples across different power cycles [7].

3. Reinforcement Methods for the Reliability of sic MOSFETs

To address the robustness challenges faced by silicon carbide (SiC) MOSFETs in practical applications, researchers have proposed several enhancement strategies. These strategies primarily focus on strengthening the GOX layer stability and reducing the boundary state density, thereby enhancing overall device performance and reliability. Key approaches include optimizing the thermal oxidation process to minimize defect formation, employing advanced materials for gate oxide layers to improve durability, and refining epitaxial growth techniques to achieve high-quality interfaces. Furthermore, methods such as post-oxidation annealing and surface passivation are being investigated to mitigate the impact of interface states. Through these comprehensive enhancements, the intent is to enhance the working lifespan of SiC MOSFETs and ensure their resilience in challenging high-power and high-temperature environments.

3.1. High-temperature oxidation process reinforcement

The high-temperature oxidation process is a highly effective technique for significantly mitigating interface defects and enhancing the uniformity of the oxide layer through treatment at elevated temperatures. For example, research by Le Huu et al. demonstrated that dry oxidation at 1450°C markedly reduces interface state density and enhances the long-term reliability of the oxide. This method optimizes the interface by minimizing residual carbon atoms and suppressing the decomposition of SiC, critical factors for maintaining interface stability.

Figure 6 depicts the DOS at the SiC/SiO2 interface below the conduction level of SiC, as determined by Hi-Lo measurement techniques across a thermal level interval between 25°C to 300°C. The data illustrates variations in the density of states over this temperature spectrum, highlighting the efficacy of high-temperature oxidation in reducing interface states. These findings underscore the importance of precise thermal management and oxidation protocols in the manufacturing of SiC MOSFETs, ensuring their durability in demanding high-heat and high-energy applications [3].

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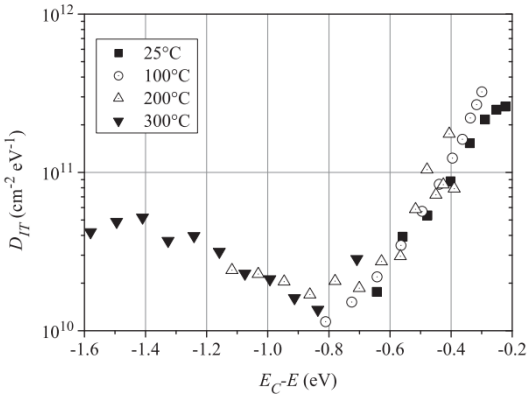

Figure 6. The DOS at the SiC/SiO2 interface, determined from Hi-Lo measurement techniques carried out over a temperature range from 25℃ to 300℃ [3]

3.2. Annealing reinforcement methods

To enhance the robustness of the GOX layer in SiC MOSFETs, understanding the effects of annealing on interface trap charge and gate dielectric stability is crucial. Dong et al. [2] investigated the impact of diluted N2O annealing duration on SiC MOS capacitors. They observed that increasing annealing duration appropriately could significantly decrease interface state density, thereby enhancing the breakdown field strength of the gate dielectric. However, prolonged annealing times might result in an increased flatband voltage shift, potentially leading to premature breakdown of the gate dielectric.

Figure 7 presents the normalized C-V curves for samples subjected to various post-oxidation annealing (POA) times, with the dashed line representing the ideal C-V curve calculated using Poisson's equation. This underscores the necessity of optimizing POA durations to balance the advantages of reduced interface states against the risk of increased flatband voltage shift, thereby improving the overall reliability of the gate dielectric in SiC MOSFETs [2].

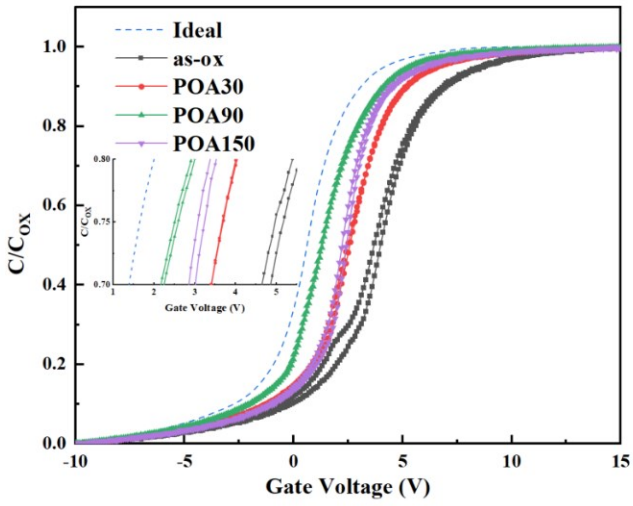

Figure 7. Normalized C-V curves for samples with varying N_2O post-oxidation annealing (POA) times[2].

3.3. Packaging reinforcement methods

Advanced packaging techniques play a crucial role in enhancing the robustness of SiC MOSFETs by effectively mitigating thermal and mechanical stress through improved materials and design. Research

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by Afanasev et al. underscores that optimizing packaging methods significantly enhances the long-term stability and reliability of SiC MOSFETs. This includes selecting materials capable of withstanding high temperatures and mechanical strain, as well as designing packages that efficiently dissipate heat and minimize stress on components.

Figure 8 depicts the cube root of internal photoemission (IPE) yield plotted against photon energy for n-type 3C (circles), 4H (squares), and 6H SiC (triangles) MOS structures, measured under an electric field strength of 3 MV/cm. Clear spectral thresholds for the three bands are indicated to aid comprehension. Additionally, the inset provides a schematic band diagram of the SiO2/SiC interface, visually representing the energy bands and interface states. This detailed analysis highlights the critical role of advanced packaging techniques in preserving the integrity and performance of SiC MOSFETs during prolonged operation, particularly in demanding environments [8].

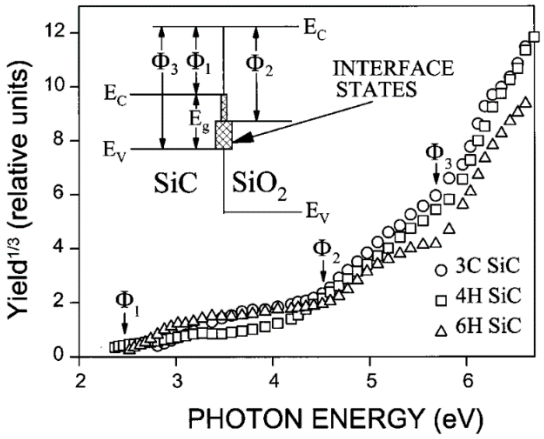

Figure 8. The cube root of internal photoemission (IPE) yield plotted against photon energy for n-type 3C (circles), 4H (squares), and 6H SiC (triangles) MOS structures measured with an electric field strength of 3 MV/cm. The spectral thresholds for the three bands are indicated for clarity. An inset shows a schematic band diagram of the SiO2/SiC interface [8].

4. Conclusion

This paper investigates the reliability challenges encountered by SiC MOSFETs in high-energy and high-heat applications, focusing on the robustness of the GOX layer and the impact of boundary state on device performance. The study reveals that in environments with elevated temperatures and electric fields, the robustness of the GOX layer in SiC MOSFETs is predominantly influenced by interface defects and the epitaxial layer quality. Early failures often stem from defects related to carbon release and traps formed during thermal oxidation, leading to local electric field concentrations and accelerated breakdown.

To address these challenges, various enhancement methods have been explored. The high-temperature oxidation process effectively reduces interface defects and enhances oxide uniformity, thereby significantly reducing the interface state density. Annealing treatments in diluted nitrous oxide (NOx) or nitric oxide (NO) atmospheres have been shown to improve interface characteristics and oxide quality, decreasing interface state density and near-interface traps. This improvement enhances gate oxide reliability and electron mobility.

Furthermore, advanced packaging techniques are employed to reduce thermal and mechanical stress, thereby enhancing the long-span stability and robustness of SiC MOSFETs. This research not only contributes new insights into enhancing the reliability of SiC MOSFETs but also lays the groundwork for the development of future high-efficiency electronic devices. By optimizing the manufacturing process of the GOX layer and improving interface characteristics, the performance and robustness of SiC MOSFETs are significantly enhanced for applications such as electric vehicles, high-frequency

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operations, and high-power density environments. These findings hold substantial implications for advancing the practical application of SiC devices across various fields.

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