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The Review of Structure Development of Gate-stacked Double-Gate MOSFETs

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Abstract. Gate-stacked double-gate (DG) MOSFETs, featuring a thin SiO_2 interfacial layer combined with high-k dielectrics, improve electrostatics, suppress leakage, and mitigate short-channel effects, enhancing the performance implication. They are promising for low-power electronics, high-performance computing, and biosensing. Conventional MOSFET scaling faces critical bottlenecks, as high-k dielectrics alone suffer from leakage and interface issues. At the same time, structural innovations such as FinFETs cannot fully suppress short-channel effects at advanced nodes. GAA demonstrates good performance, but costs excessively. This work innovatively proposes co-optimizing materials (Al_2O_3, HfO_2, La_2O_3) and structures (strain engineering, dual-material gates, multigate topologies) in gate-stacked double-gate (DG) MOSFETs, integrating high-k stacks with multigate architectures to reinforce electrostatics and scalability. Such synergy ensures enhanced performance while meeting the dual demands of low-power electronics, high-performance computing, and emerging biosensing applications.

Keywords: Gate-stacked double-gate MOSFETs, high-κ dielectrics, short-channel effects, low-power electronics.

1. Introduction

MOSFETs are integrated circuits' fundamental building blocks, essential in switching and amplifying virtually all digital logic, memory, and analog systems. Their compact dimensions and low power consumption have long driven the continuous scaling of very large-scale integration (VLSI). However, as device geometries shrink to 5 nm and below, conventional single-gate MOSFETs encounter pronounced limitations, including severe short-channel effects (SCEs), increased leakage currents, and diminished gate electrostatic control [1].

To overcome these challenges, multigate device architectures such as double-gate (DG), FinFET, and gate-all-around (GAA) MOSFETs have been developed [2]. The DG-MOSFET can be recognized as a transitional stage between single-gate MOSFETs and FinFETs. DG MOSFETs are irreplaceable because of the mature technology, low cost, and energy conservation, which means they are essential in low-power circuits. If they overcome challenges by redesigning their structure, the DG MOSFETs can be cheaply applied to more demanding circuits. Furthermore, two gates perform better for enhancing electrostatic control of the channel [3], with recent studies demonstrating notable suppression of short-channel effects (SCEs) through the integration of two-

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dimensional materials [1]. Based on DG MOSFETs' structure, variants such as DMDG MOSFETs, strained DG MOSFETs, and gate-stacked DG MOSFETs have been proposed to refine threshold voltage control further, improve subthreshold swing, and so on [4, 5]. Within this framework, gate-stacking—using a multilayer dielectric stack instead of a single SiO_2 layer—has become a central research focus. This review concentrates on gate-stacking, particularly emphasizing how material innovations and device engineering can be leveraged to optimize its performance further.

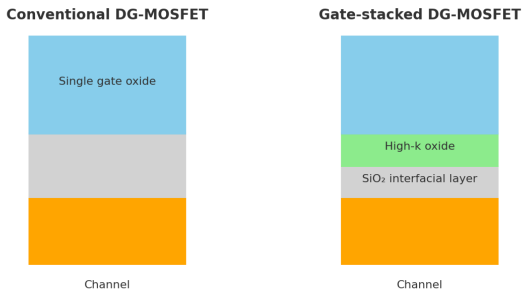

Figure 1. The difference between conventional DG-MOSFET and Gate-stacked DG-MOSFET. Left: conventional DG-MOSFET with a single gate oxide. Right: gate-stacked DG-MOSFET employing a SiO_2 interfacial layer and a high-k dielectric layer, which enhances gate control and suppresses short-channel effects

As illustrated in Figure 1, it is clear that gate stacking typically combines a thin SiO_2 interfacial layer with a high-k dielectric, simultaneously preserving interface quality and enhancing gate control [6, 7]. This approach benefits logic circuits and extends to biosensing and ultra-low-power applications [8,9]. Moreover, studies on trigate and nanowire-based devices suggest further opportunities through integrating structural and material engineering [10,11].

Current research faces scaling challenges: although FinFETs alleviate short-channel effects (SCEs), they cannot fully suppress them at deeply scaled nodes [2]. At the same time, gate-all-around (GAA) transistors offer superior electrostatic control but incur excessive fabrication cost and complexity. The gate-stacking structure has been introduced to address these issues and enhance DG-MOSFETs' performance [3, 6]. Nevertheless, reliance on a single technological approach remains insufficient. While gate-stacking effectively mitigates SCEs and improves device characteristics, it cannot be absolutely eradicated and simultaneously introduces new challenges, including elevated interface trap density and band alignment concerns [12, 13].

Considering these factors, this review introduces the structural development of gate-stacked DG-MOSFETs, evaluating their capability to suppress SCEs, and addressing their inherent limitations. Distinct from prior surveys, we emphasize the innovative perspective that further progress relies on integrating gate-stacking with complementary optimization strategies, including exploring diverse high-k dielectrics, incorporating strain engineering, and adopting dual-material gate concepts [14]. Such synergistic approaches strengthen the intrinsic benefits of gate-stacking and provide new avenues to refine threshold voltage control, enhance subthreshold swing, and boost device scalability. Building on structural advances and material/process innovations, this review outlines a roadmap toward more stable, energy-efficient, and versatile DG-MOSFET platforms for next-generation CMOS technologies [10, 11].

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2. Evolution of gate-stacking structures

2.1. Gate-stacking concept

As MOSFETs scaled down to the nanoscale, traditional gate structures—once sufficient at larger dimensions—became inadequate for controlling channel conduction. With channel lengths approaching the scale of depletion regions, SCEs emerged [1, 6].

In single-gate MOSFETs, this lowers source barriers, allowing carrier injection even in the "off" state, which increases leakage current, raises static power consumption, and degrades logic state distinction [7,12,13]. Strengthening electrostatic control is thus critical to suppress drain-induced barrier lowering (DIBL) and related SCEs. Double-gate (DG) MOSFETs mitigate these issues using two gates to enhance gate–channel coupling [3,4,11]. However, residual SCEs and reliability challenges remain. To further enhance control, DG-MOSFETs have evolved to adopt gate-stacked dielectric structures, incorporating multilayer dielectrics for improved electrostatic performance [6, 7].

Compared with conventional DG MOSFETs, gate-stacked DG MOSFETs differ in the gate dielectric by adding a high-k layer on top of SiO_2 [5,6,10]. Because a high-k material is more easily polarized, the equivalent oxide thickness (EOT) becomes smaller than that of SiO_2 at comparable physical thickness. Viewing the gate, gate dielectric, and channel as a capacitor, C_{ox} follows the same relation:

$$C_{ox} = \frac{\varepsilon A}{tox} \tag{1}$$

which directly links larger permittivity (high-k) or smaller effective thickness (EOT) to a higher C_{ox} [6, 10].

By analogy with a parallel-plate capacitor, an increase in the gate-oxide capacitance C_{ox} leads, for a given gate voltage V_{GS} , to a larger induced inversion charge in the channel. Consequently, the channel carrier density and the drain current I_D increase; this effect is often accompanied by a reduction in the device threshold voltage Vth, producing several practical advantages.

A lower V_{th}enables the transistor to switch on at a smaller gate voltage (V_{gs}), establishing the conducting channel earlier during a voltage ramp. Since DG MOSFETs are central to low-power applications, gate-stacking further enhances their compatibility with such circuits by improving electrostatic control. Additionally, the increased drive current in the on-state strengthens timing margins and operational robustness, particularly critical under low V_{DD} conditions.

This expression captures these relationships:

$$I_D \approx \mu \cdot C_{ox} \left(W/L\right)(V_{gs} - V_{th})^2 \tag{2}$$

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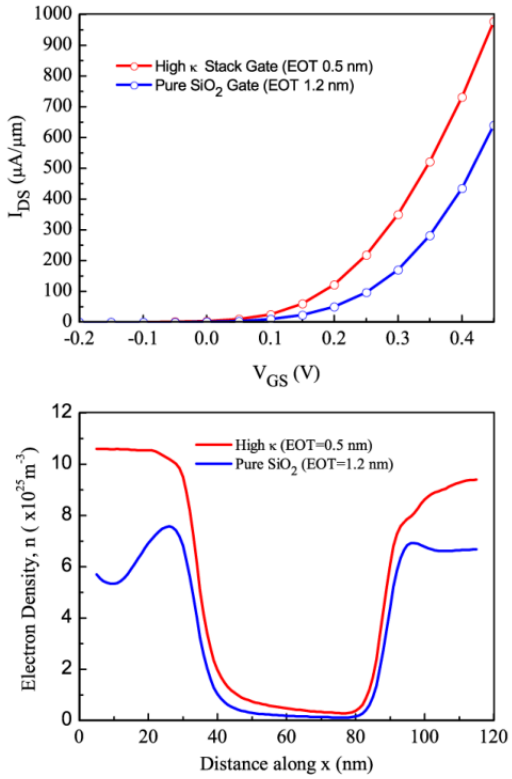

Figure 2. Electron density and distance along x for V_{DD} [6]

(a) The high-κ stack (EOT = 0.5 nm) exhibits higher I_{on} than pure SiO_2 (EOT = 1.2 nm), indicating enhanced drive current and reduced V_{th} due to increased C_{ox}.

(b) Electron density along the channel is higher in the high-κ stack device, confirming improved gate control.

Figure 2 demonstrates the core mechanism: EOT ↓ ⇒ C_{ox}↑ ⇒ V_{th}↓ ⇒ I_{on}↑, supporting the performance advantage of gate-stacked DG-MOSFETs.

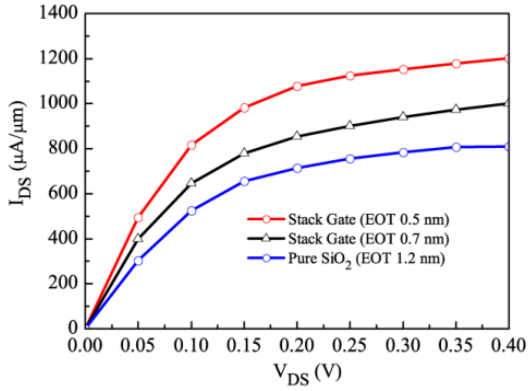

Figure 3. I_{DS}–V_{DS} Characteristics of DG-MOSFETs with different EOTs [6]

In Figure 3, V_{th} decreases as EOT reduces from 1.2 nm (SiO_2) to 0.7 nm and 0.5 nm (high-κ stacks), confirming stronger gate control.

Despite the advantages of high-κ materials, a thin SiO_2 interfacial layer is typically retained to address challenges such as high interface-state density, poor band alignment with silicon, and

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process immaturity [7,10]. Band alignment is critical for minimizing gate leakage and ensuring device reliability. SiO_2 provides favorable conduction and valence band offsets, effectively suppressing unwanted carrier tunneling [6,7], which explains its continued use as a foundational layer in gate-stacked DG-MOSFETs that shows evidently in Figure 4. This integration balances high-κ dielectrics' benefits with traditional interfaces' stability, forming a key part of current optimization strategies.

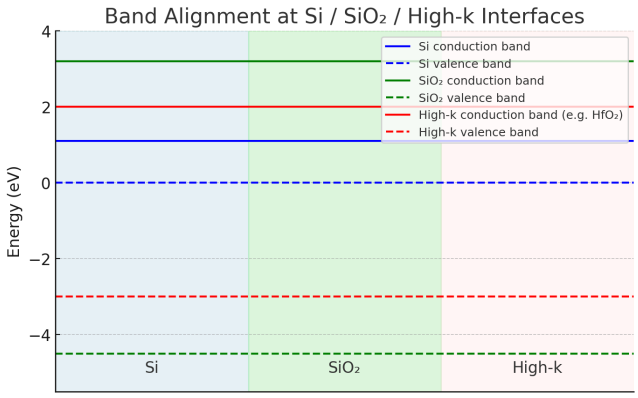

Figure 4. The high band alignment between Si and SiO_2 and the low band alignment between Si and the high-k material

Above all, gate stacking has proven highly effective in mitigating short-channel effects by reducing EOT, enhancing gate capacitance and drive current, and lowering the threshold voltage. However, further optimization remains possible, particularly in addressing performance limitations through improved material selection and structural engineering. The following section focuses on analyzing key performance metrics to identify critical factors and guide the development of more efficient and reliable gate-stacked DG-MOSFETs.

2.2. Material choices

Several viable high-k dielectric candidates exist, including HfO_2, Al_2O_3, ZrO_2, and La_2O_3. As noted earlier, the primary selection criterion is the ability to reduce the equivalent oxide thickness (EOT) while maintaining acceptable leakage. In a study by Farzana et al. [6], the optimal gate-stacking structure was investigated using a quantum ballistic transport model. Their work focused on a fully depleted n-type DG-MOSFET, with the top gate employing a SiO_2/La_2O_3 stack, a 4 nm bottom oxide, and an intrinsic silicon channel. The source/drain doping was set to 2×10^{20} cm^{-3}, the silicon film thickness to t_{Si}=2.5 nm, and the metal gate work function to 4.2 eV.

Furthermore, Salmani-Jelodar et al. [7] stressed that, for a fixed EOT = 0.86 nm, the optimum interface oxide thickness depends on the dielectric constant of the high-k layer: Al_2O_3 requires ≈3 Å SiO_2, HfO_2 ≈5 Å, and La_2O_3 ≈7 Å to balance leakage suppression and electrostatic control.

For comparison, the minimum usable top oxide thickness in a conventional SiO_2-only device is about 1.2 nm, below which gate tunneling becomes prohibitive. By contrast, high-k gate stacks achieve much smaller effective EOT values (≈0.7–0.5 nm, as derived from equations (3)) without sacrificing leakage performance, owing to their larger physical thickness.

$$t_{phys} = \frac{\kappa_{h_i}}{\kappa_{ox}} \times EOT \tag{3}$$

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Table 1. Performance comparison of different high-k materials (EOT = 0.86 nm, based on [7])

High-k Material	Recommended SiO_2 Interfacial Layer	I_{ON} (Drive Current)	I_{OFF} (Leakage Current)	SS (Subthreshold Swing)	DIBL	I_{Gate} (Gate Tunneling)	Overall Assessment
Al_2O_3 (k≈9)	≈ 3 Å	Moderate to high, good drivability	Very low, best among candidates	Close to ideal	Well suppressed	Extremely low	Most balanced, suitable for low-power applications
HfO_2 (k≈ 20)	≈ 5 Å	High, significant improvement	Well controlled	Slightly higher than Al_2O_3	Relatively low, slight degradation	Low	Balanced choice, mainstream for high-performance nodes
La_2O_3 (k≈ 30)	≈ 7 Å	Highest, strongest drivability	Relatively high, leakage concern	Noticeably degraded (due to thickness)	Poor performance	Low	Suitable for extreme scaling exploration, but with reliability concerns

As shown in Table 1, different high-κ dielectric materials present distinct trade-offs among drivability, leakage suppression, and short-channel control. Given that double-gate (DG) MOSFETs are predominantly used in low-power circuit applications, materials with low leakage currents and mature fabrication compatibility are particularly desirable. From this perspective, Al_2O_3 combined with a SiO_2 interfacial layer emerges as an optimal choice. This stack offers the most balanced characteristics, including near-ideal subthreshold swing (SS), extremely low gate tunneling current, and excellent electrostatic control, making it especially suitable for ultra-low-power applications and thus well aligned with the inherent advantages of DG MOSFETs.

Moreover, considering the potential for DG MOSFETs to be extended into HPC domains with reduced cost, HfO_2 and La_2O_3 present promising opportunities. Although La_2O_3 raises concerns related to interface reliability and increased leakage, its exceptionally high drive current indicates strong potential for performance-critical nodes with DG MOSFETs. These drawbacks may be addressed through complementary techniques, such as strain engineering and dual-material gate (DMG) integration, which have improved carrier mobility and electrostatic integrity.

2.3. Other promising structural optimization strategies

Beyond material selection, strain engineering and dual-material gate (DMG) design offer effective structural enhancements for gate-stacked DG-MOSFETs. Strain engineering improves carrier mobility by reducing effective mass, enhancing drive current, a critical advantage for high-speed and high-performance logic applications [5]. In parallel, the DMG structure introduces a step potential along the channel using two gate materials with different work functions, suppressing short-channel effects such as DIBL while enabling threshold voltage tuning without degrading drivability [4].

When combined with gate stacking, both techniques address complementary challenges. While gate stacking strengthens gate control and suppresses leakage and strain, DMG improves current transport and electrostatic modulation. This co-optimization boosts device performance and expands DG-MOSFET applicability—from low-power circuits to performance-driven systems and emerging domains like biosensing [7].

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Table 2. Synergistic design strategies for high-performance/low-power MOSFET structures

Module	Recommended Structural Combination	Synergistic Mechanism
Channel Region	Tensile strain (for nMOS) / Compressive strain (for pMOS)	Enhances carrier mobility
Gate Dielectric	SiO_2 / HfO_2 stack (Gate-stacked structure)	Reduces leakage, strengthens electrostatic control
Gate Metal Layer	TiN (source-side) / TaN (drain-side) — DMG structure	Tailors potential distribution, suppresses DIBL
Overall Objective	High I_{on}, low I_{off}, strong gate control, low power consumption	Ideal for high-performance/low-power SoC core applications

In Table 2, there are optimized structural strategy for gate-stacked DG-MOSFETs combining strain and DMG to enhance mobility, gate control, and short-channel suppression for advanced CMOS applications.

3. Performance optimization of gate-stacked double-gate MOSFETs

Building on the structural advantages of gate-stacked DG-MOSFETs, assessing how these design choices translate into measurable device performance is necessary. Key figures of merit—such as the on-state current (I_{on}), off-state leakage (I_{off}), subthreshold swing (SS), and drain-induced barrier lowering (DIBL)—provide critical insight into the trade-offs between enhanced gate control and potential reliability challenges.

3.1. Improved subthreshold characteristics

The subthreshold swing (SS) in gate-stacked DG-MOSFETs can be significantly reduced—approaching the theoretical limit of ~60 mV/dec—thanks to enhanced gate electrostatics [6,7]. This improvement effectively suppresses short-channel effects and mitigates threshold voltage variation, enabling steeper switching characteristics [12], because

$$SS = \frac{dV_{GS}}{d(\log I_D)} \approx \ln\left(10\right) \times \frac{kT}{q}\left(1 + \frac{C_{dep}}{C_{ox}}\right) \tag{4}$$

Such behavior is essential for low-power design, supporting reliable operation at reduced supply voltages. By achieving near-ideal SS through gate-stacking, these devices offer a compelling route toward energy-efficient CMOS technologies with potential applications in biosensing and ultra-low-power systems [8].

Regarding gate-stacking structure, high-κ gate stacks improve gate control, lowering the subthreshold swing from 74 mV/dec to 63 mV/dec [6] compared to conventional SiO_2 gates. Together, these results substantiate the logical chain: EOT ↓ ⇒ C_{ox}↑ ⇒ V_{th}↓ ⇒ I_{on}↑,

A key aspect yet to be fully explained is how an increased gate oxide capacitance C_{ox} contributes to lowering the V_{th}.

$$V_{th} \approx V_{fb} + 2\phi_f + \frac{\sqrt{2\varepsilon_{Si} q N_A 2\phi_f}}{C_{ox}} \tag{5}$$

This formula can actually expound the logic there.

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Among these, lowering V_{th} also increases the transistor's sensitivity in the subthreshold region: the device responds more strongly to small changes in gate voltage. This property can be exploited in ultra-low-power sensing applications (e.g., biosensors) to improve sensitivity and detection accuracy [8].

3.2. Reduced leakage current

Reducing leakage current can help us improve the performance of the MOSFET in our design and optimization. More specifically, the tunneling current accounts for a significant proportion of the leakage current, which is the kernel problem for the gate-stacking structure to address.

As stated before, when the gate dielectric is replaced with the high-k material, the EOT declines, but physical thickness augments [6], which addresses the tunneling current. In that way, the tunneling current will nearly disappear when the dielectric's physical thickness is enough.

$$Trans \approx exp\left[-2\sum_i T_i P_i\right] \tag{6}$$

If the SiO2 layer's thickness is less than 1.2nm, electrons will penetrate the whole layer, and the tunneling current will dominate.

Another essential part of the leakage current is the subthreshold current. Among the various leakage components in scaled MOSFETs, the subthreshold current is often dominant, especially when the gate voltage is below the threshold voltage. In this regime, carriers are still thermally activated to overcome the potential barrier, giving rise to an exponential dependence of the drain current on the gate bias:

$$I_{sub} \approx I_0 exp\left(\frac{V_{Gs}-V_{th}}{nV_T}\right) \tag{7}$$

A steeper subthreshold swing (SS) therefore suppresses subthreshold leakage by reducing the slope of this exponential relationship [7]. Due to their enhanced gate control and reduced EOT, gate-stacked DG-MOSFETs effectively lower subthreshold leakage compared with single-gate counterparts [6]. This improvement reduces static power consumption and enables reliable operation in low-power circuits and sensing applications, where leakage currents are critical design constraints [8].

3.3. Increased drive current (Ion)

As discussed earlier, enhancing the drive current (I_{on}) is a core motivation behind adopting gate-stacked structures in DG-MOSFETs. By reducing the equivalent oxide thickness (EOT), high-κ dielectrics increase the gate capacitance (C_{ox}), which directly strengthens the gate–channel coupling and enables more carriers to flow during the on-state. Physically, I_{on} represents the current conducted by electrons or holes per unit time when the device is active—thus, a higher drive current implies faster charge/discharge cycles within the transistor.

At the circuit level, switching delay is inversely proportional to I_{on}, as expressed by

$$\tau \approx C_{load} V_{DD} / I_{on} \tag{8}$$

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Therefore, increasing I_{on} reduces delay and enhances switching speed, improving operating frequency and logic throughput. Simulations based on quantum ballistic transport [6] reveal that decreasing the EOT from 1.2 nm to 0.5 nm using high-κ stacks leads to a 48.68% increase in I_{on}, demonstrating the efficacy of this approach in performance scaling.

Furthermore, strain engineering can be integrated to reduce carrier effective mass and boost mobility [5], providing an additional pathway to enhance I_{on}. High-performance computing (HPC) applications benefit significantly from such improvements, where rapid logic switching is essential. Meanwhile, in ultra-low-power domains, a higher I_{on} under constant V_{DD} helps reduce energy per operation, aligning with energy efficiency goals [9].

4. Application fields of gate-stacked double - gate MOSFETs

Gate-stacked DG-MOSFETs, benefiting from enhanced gate control and reduced leakage, present a highly adaptable platform for low-power and high-performance applications. In ultra-low-power electronics, suppressing subthreshold swing and gate leakage enables reliable operation at reduced supply voltages, making these devices ideal for battery-constrained systems, such as portable electronics and IoT sensors [6,7,9]. Simultaneously, when integrated with strain engineering, gate-stacked DG-MOSFETs achieve significant improvements in carrier mobility and drive current, offering a cost-effective solution for high-performance computing (HPC) scenarios that demand rapid charge/discharge cycles and high-speed logic switching [5].

Beyond digital logic, their steep subthreshold characteristics make them well-suited for biosensing applications, where sensitivity to minute voltage changes is critical for detection accuracy. For example, Singh et al. [8] demonstrate that gate-stacked configurations significantly enhance biosensor transduction efficiency by amplifying low-amplitude signals. Moreover, gate-stacking compatibility with emerging multigate architectures—such as FinFETs and GAAFETs—ensures continued relevance in advanced technology nodes, facilitating scalable CMOS integration.

Looking forward, the optimization of gate-stacked DG-MOSFETs demands the selection of high-κ materials with favorable electrostatic and leakage characteristics and synergistic co-design strategies. These include integrating strain engineering, dual-material gates, and structural innovations like FinFET or DMDG architectures [4,5], which mitigate reliability issues such as interface trap density or band misalignment. While Al_2O_3 gate stacks offer a balanced solution for low-power use cases, HfO_2 and La_2O_3 variants unlock potential in performance-driven systems, albeit with trade-offs that require advanced co-optimization [7].

5. Future development trends of the gate-stacking structure

While gate-stacked DG-MOSFETs have shown impressive gains in short-channel control and leakage suppression, further refinements are needed to meet the demands of scalable and application-specific design. One critical direction is the judicious selection of high-κ materials for gate stacks. For instance, Al_2O_3 with a SiO_2 interfacial layer strikes an optimal balance—offering low leakage, ideal subthreshold swing, and compatibility with ultra-low-power logic, making it especially suitable for DG-MOSFET deployment in power-sensitive domains. Additionally, the dielectric stack must continue to evolve to address reliability and integration issues such as band alignment and interface quality.

Beyond materials, co-design strategies combining gate-stacking with strain and dual-material gate (DMG) techniques offer a path toward performance-driven customization. Strain enhances mobility; DMG improves potential distribution and suppresses DIBL; gate-stack boosts C_{ox} and

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suppresses leakage. These effects align well with emerging application demands: for example, HPC circuits require high drive current and fast switching—both achievable via strained high- C_{ox} stacks. Combining with material, La_2O_3, while presenting reliability and leakage challenges, stresses outstanding drive current, highlighting its potential in high-performance DG-MOSFET designs. Meanwhile, ultra-low-power designs benefit from steeper subthreshold slopes and lower V_{th}, realized through gate-stack–DMG synergy. In biosensing, the sharp SS directly enhances detection sensitivity. Future development should thus focus on integrated material–structure strategies.

6. Conclusion

This work systematically reviews the structural and material evolution of gate-stacked double-gate (DG) MOSFETs as a response to the scaling limits of conventional single-gate devices. By introducing stacked high-k/SiO_2 gate dielectrics, these transistors achieve reduced leakage, enhanced electrostatics, and improved figures of merit such as subthreshold swing, drain-induced barrier lowering, and drive current. Their applicability spans low-power circuits, high-performance computing, and biosensing, underscoring both breadth and technological relevance. Despite unresolved issues in interface quality, band alignment, and scalability at deep nanoscale nodes, the study stresses that gate-stacked DG-MOSFETs form a critical stepping stone toward next-generation CMOS. Their value lies in immediate performance benefits and compatibility with advanced architectures, ensuring a continuous pathway for semiconductor innovation.

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