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Design of ECG circuits for wearable devices

Guang Wu

Zhongyuan-Petersburg Aviation College, Zhongyuan University of Technology, Zhengzhou, China, 450007

202028024223@zut.edu.cn

Abstract. Heart diseases have become more and more prominent in recent years. ECG signals can accurately reflect the health of hearts during the detection process. The use of wearable ECG devices requires low power consumption, a high common-mode rejection ratio, and minimal noise. Traditional research has concentrated on lowering the circuit's overall power dissipation, which typically results in less current flowing through the amplifier but higher circuit noise. Therefore, this places higher demands on the amplifier in the circuit. Electronic devices are becoming smaller due to the rapid development of semiconductor technology. Amplifiers designed for semiconductor devices can effectively solve the problems mentioned above. The circuit created in this study has a low power need, a high common-mode rejection ratio, is compact, has a high input impedance, and has a low input-referred noise level. In addition, LT-Spice software was used to design and simulate the circuit, and the results were analyzed and calculated accordingly. The circuit meets the requirements of the project design. The frequency range of the circuit is 1mHz - 227.9Hz. The differential gain of the circuit is 36.6dB. The integrated input-fred noise is 3.94uV. The total consumption of electricity is 4.67W. These data indicate that the circuit has a high gain in the frequency range of ECG signals, which can filter out other interference signals. It also solves the problems of power consumption and noise.

Keywords: Wearable ECG Devices, Low Noise, Low Power Consumption, High Common-Mode Rejection Ratio.

1. Introduction

The frequency of heart disease has greatly increased in recent decades. Every year a large number of people die of heart disease. This is caused by many people being obsessed with electronic devices as well as eating some harmful foods. Cardiovascular disease is also linked to socioeconomic status and medical conditions [1]. Any biological activity is necessarily related to bioelectricity. Through bioelectric models, people know the problems of the body and can adjust and treat them in a targeted manner [2]. Electrocardiogram (ECG) equipment makes use of this principle. With the increasing incidence of heart disease, universal ECG is necessary because it allows patients to detect diseases in advance [3]. However, heart disease is often unpredictable. This puts some demands on the designed equipment. This means that such devices must detect the state of the heart in real time. Observing premature contractions requires ECG equipment to have the ability to be used for a long time (from 24 hours to 14 days) [4]. Then, although some equipment in the hospital has relatively high accuracy, its large size is not conducive to continuous detection [5]. This requires that the designed ECG equipment must have the characteristics of low power consumption and small size. To solve this set of problems,

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complementary metal oxide semiconductor (CMOS) tubes are added to the design process. This project also makes use of traditional 3-op-amp circuits. At the same time, the amplifier designed by the CMOS tube is used as an amplifier in the traditional 3 Operational Amplifier (3op-amp) circuit. In this way, the volume problem of traditional equipment can be effectively solved. In the design of wearable ECG devices, Ma proposed an approach. The circuit design was based on the characteristics of the subthreshold circuit and the design requirements of the ECG signal acquisition circuit. It has the characteristics of low power consumption and small size [5]. Wang proposed a digital-analog hybrid electrode that compromises noise and power consumption. When the system noise is low, the use of chopping technology also gives the system a higher input impedance [6]. In terms of noise, Ma et al. proposed a chopping technique and transistor noise optimization technology. By using this design, the circuit's input impedance is increased and its noise is decreased [7]. Li proposed a chopper-type analog front end with low power consumption and strong anti-interference. The project's input noise is 4.5uV, the power consumption is 1.2uW, and there is a common-mode rejection ratio of 118dB [8]. It can be seen that the noise level is also very important for the signal acquisition of wearable devices. This project provides a new solution by adding a right-leg drive circuit to the traditional 3-op-amp circuit. The last amplification stage of the 3OP-amp circuit and the right-leg drive circuit form a common-mode extraction circuit. By using this method, the common-mode rejection ratio can be increased and noise levels in the circuit can be reduced.

2. Method

This project determines the performance indicators of circuit design through some past research. At the same time, some traditional circuits were improved according to the indicators. Let the entire circuit meet the design needs.

2.1. Requirements for design metrics

(1) Bandwidth: In order to reduce noise, the bandwidth range is set from 1mHz-250Hz to filter out part of the noise without losing the ECG signal.

(2) Gain: Because the ECG signal amplitude is 100uV-5mV, in order to put it to a large observable amplitude, the gain needs to be hundreds or thousands of times. So, this project sets the gain to around 40dB [5].

(3) Total integrated input-referred noise: Due to the low frequency and small amplitude of the ECG signal, it is easily interfered by noise. So, the acquisition circuit should not have high noise. According to the ANSI-13 standard given by the American National Standards Institute (ANSI), the input noise is recognized as 4.03uV. Therefore, the input noise of this project is less than 4uV [5].

(4) power consumption: Generally speaking, the power consumption of most wearable devices is about tens of microwatts. In order to better reduce power consumption, this project sets the power consumption below 5uW [5].

According to traditional research and the characteristics of human ECG signals, the ECG amplifier in this project must, at minimum, meet the following specifications:

- Frequency range: 0.1Hz – 250Hz ± 10%
- Differential gain: 40dB ± 5dB
- Total integrated input-referred noise: <4μVRMS
- Total power consumption of all blocks: <5μW

The entire circuit is improved on the traditional 3 op-amp. The circuit is mainly composed of a mannequin circuit, a traditional 3op-amp, a right-leg drive circuit, and a filter circuit. The circuit's overall structure diagram is shown in Figure 1. To meet the design requirements, the signal generated by the mannequin circuit is amplified and filtered. Ling proposed a similar model with an ECG signal circuit consisting of an amplification circuit and a right-leg drive circuit [9]. The circuit structure of Figure 1 has three main advantages: 1). It defines the common-mode input range of the instrumentation amplifier. 2). Reduced common-mode noise.3). A safer way to ground the body is used, especially when

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using the current-limiting resistor R. Stage 1 consists of X5 and X2 and Stage 2 consists of X3. Stage 1 and stage 2 form a 3-op amp circuit.

Stage 1:

$$\mathrm{A_{v,dm}} = 1 + \frac{500\mathrm{k} + 500\mathrm{k}}{10\mathrm{k}} = 40\mathrm{dB} \tag{1}$$

Stage 2:

$$A_{V,dm} = -\frac{6.36}{2 \times 6.36} - \frac{6.36(6.36 \times 6.36)}{2 \times 6.36(6.36 + 6.36)} = 0dB \tag{2}$$

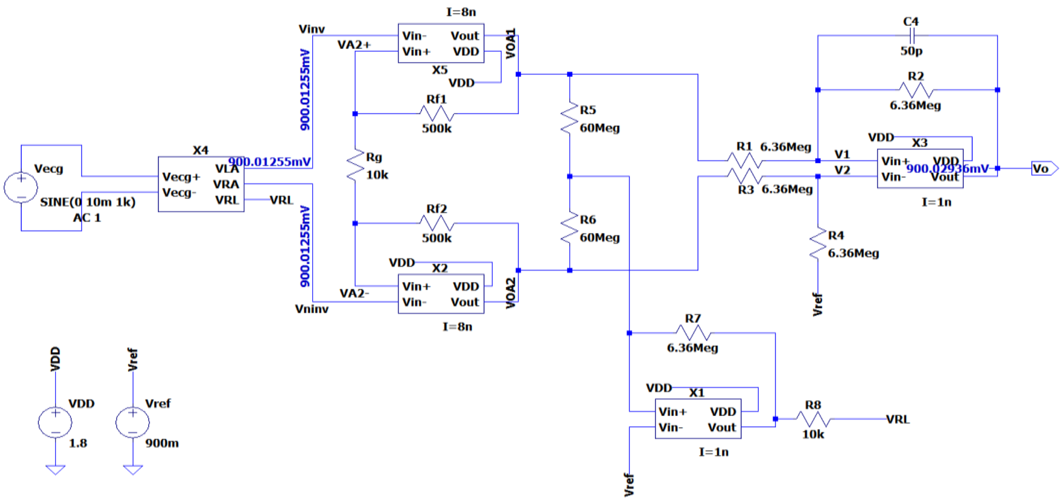

Figure 1. Diagram of the overall circuit.

2.2. *Design of the Amplifier*

The design of semiconductor amplifiers is the key to whether the project can meet the requirements. The circuit should have the characteristics of low noise, low power consumption, and a high common-mode rejection ratio (CMRR). So, amplifier for this project is based on the Berkeley Short-channel IGFET Model 180nm CMOS model. The operational transconductance amplifier has a small size, low power need, low input reference noise, and high input impedance as its distinguishing features. This circuit puts the CMOS in a subthreshold state, ensuring the continuity of the entire circuit. The amplifier circuit is shown in Figure 2. All amplifiers in this project are structured as shown in Figure 2.

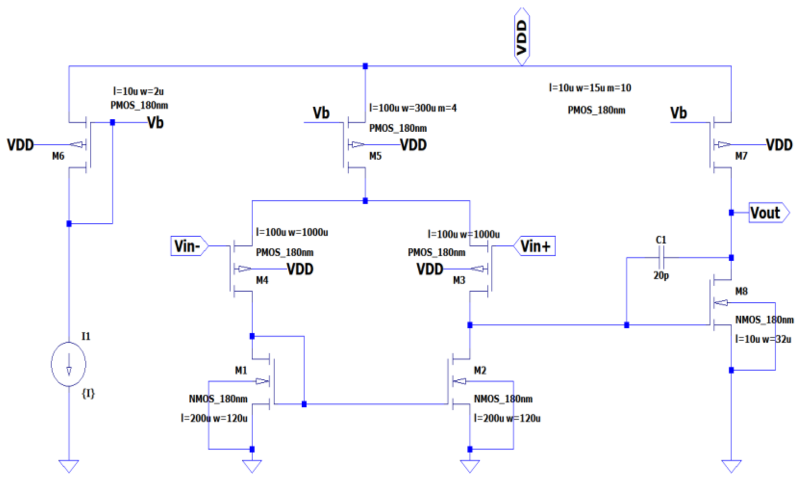

Figure 2. Operational transconductance amplifier.

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2.3. Body Simulation

Because in practical applications, most of the signals detected by this project are biomedical signals. This ECG signal is very low in frequency and very weak and also becomes susceptible to interference. For example, signal interference generated during biological movement or signal interference between Electro-Magnetic Generator (EMG) and ECG in living organisms. In this project, LT-Spice is used to design a mannequin circuit to send out human simulation signals according to the characteristics of human ECG signals. Figure 3 shows the circuit schematic for this circuit. Signal interference generated by body electrodes with resistance is reproduced by this circuit. To approximate the electrical resistance of the human body, three 200-ohm resistors are utilized. A signal with a 60Hz frequency of 0.1uA is also added to interfere with the human body.

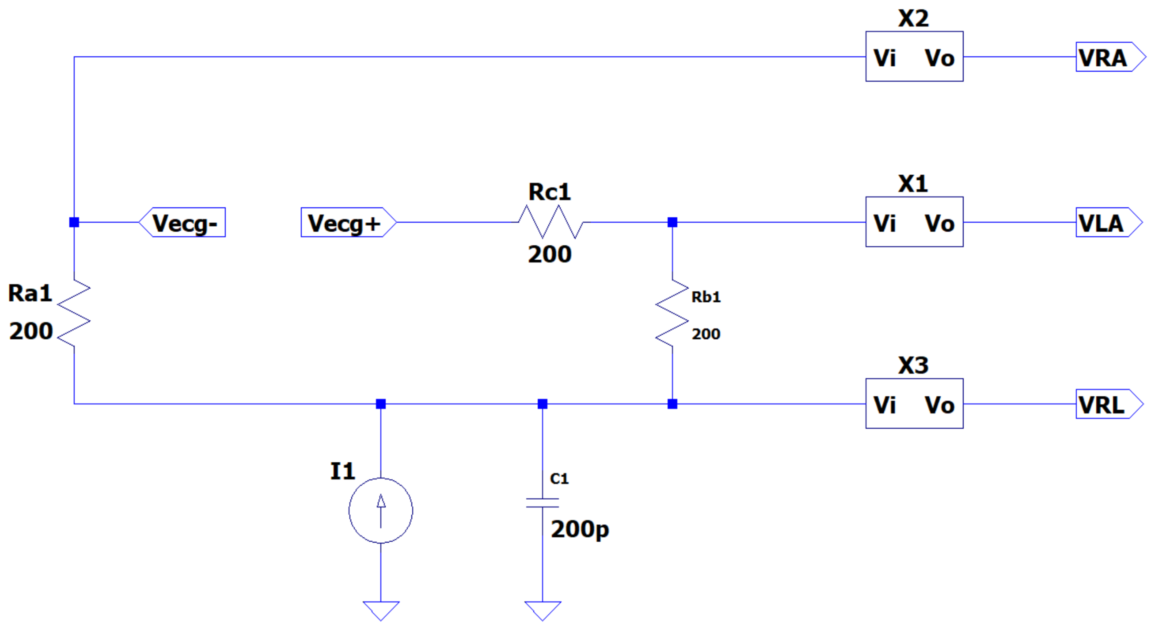

Figure 3. Human circuit model.

2.4. Filter Circuit

The ideal waveform is obtained by adding a low-pass filter in the final part of the circuit. The cutoff frequency of this circuit is 0.1Hz, based on the previous mannequin circuit's design and the characteristics of human body signals in life. As shown in Figure 4, the low-pass section consists of a resistor and a capacitor. The frequency of this circuit is determined by both the size of the capacitance and the size of the resistance. According to the requirements, the maximum frequency is about 250Hz. Therefore, the capacitance and resistor size in the circuit are set to meet the design requirements. The calculation process is as follows:

LPF:

$$f_H = \frac{1}{2\pi \times 6.36M \times 100p} = 250Hz \tag{3}$$

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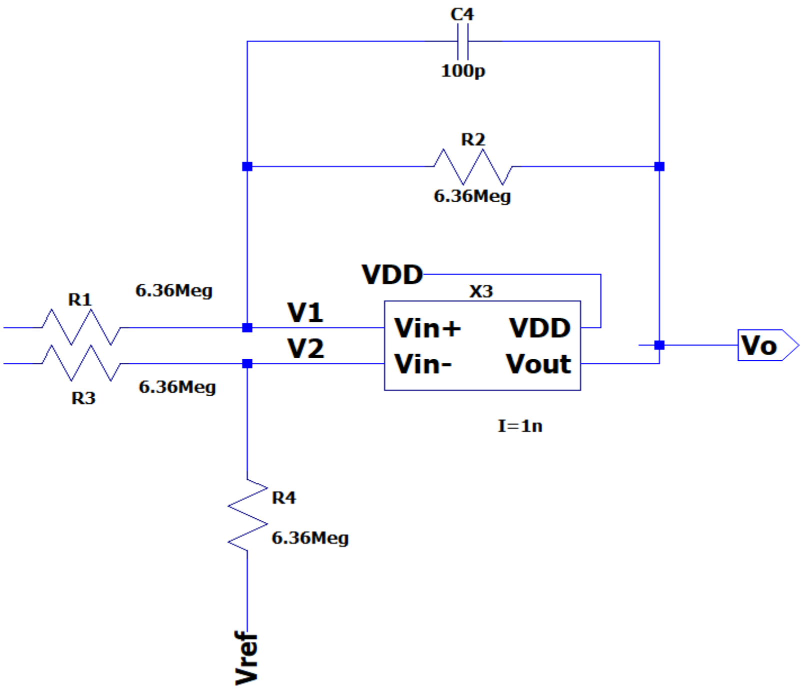

Figure 4. low-pass filter.

3. Results and Discussions

Table 1 compares the project's parameters, as determined by the LT-Spice software simulation, with the values required in real life. Simulation shows that the frequency range of the circuit is between 1mHz-258.7Hz.

The circuit is characterized by low electricity consumption, high CMRR, and low input noise. Therefore, by calculating, the CMRR size of the circuit can be calculated, and the result is as follows:

$$A_{id} = 36.5\text{dB} = 66.83 \tag{4}$$

$$A_{cm} = -76 + 45 = -31\text{dB} = 0.021 \tag{5}$$

$$\text{CMRR} = \frac{A_{id}}{A_{cm}} = 3182 \tag{6}$$

Table 1. Performance compared with requirements.

	Frequency range	Differential gain	Total integrated input-referred noise	Total power consumption	Total amount of employed capacitance
Design requirement	0.1Hz – 250Hz ± 10%	40dB ± 5dB	<4µVRMS	<5µW	< 1nF
circuit performance	1mHz-225.1Hz	36.6	3.94uV	4.67uW	100p

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3.1. Analysis of the Simulation Results

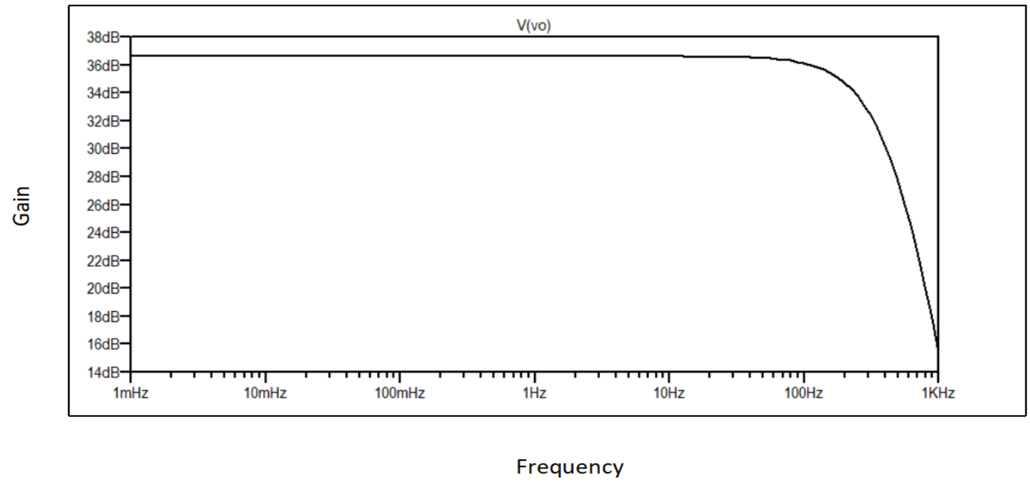

Figure 5. AC simulation results.

The first item is AC scanning from 1mHz to 1000Hz. This simulation shows the magnitude of the bandwidth and gain of this project and the relationship between them. The gain of the overall circuit is 36.6dB at the beginning, and the gain of the circuit is 34dB when the frequency is increased to 225Hz. When the frequency is between 1mHz and 1000Hz, the gain of the circuit is maintained between 36.6dB and 34dB. It meets the requirements of the project for frequency and gain.

The second simulation is to scan and draw images of noise from 1mHz to 10kHz.The output noise of the circuit is measured by LT-spice. Figure 6 displays the image of the test results. The examination of the output noise of the complete circuit is shown in Figure 6's simulation results. The total output reference noise size of the entire circuit can be observed by measuring the image as 248.38uV. This simulation result is obtained by measuring the output noise of the entire circuit. In this project, the input-referred noise is equal to the output-referred noise divided by the differential-mode gain of the circuit. The calculation shows that the total comprehensive reference input noise is equal to 3.94uV. In addition to the initial calculation, the noise efficiency factor (NEF) of the circuit can be calculated, and the calculation process follows:

Noise efficiency factor(NEF):

$$\mathrm{NEF} = V_{n,in,RMS}\sqrt{\frac{I_{tot}}{\phi_t * 4KT * BW8 * \frac{\pi}{2}}} = 15.8\ (\ K = 1.38 \times 10^{-23}\ T = 298 \qquad (7)$$

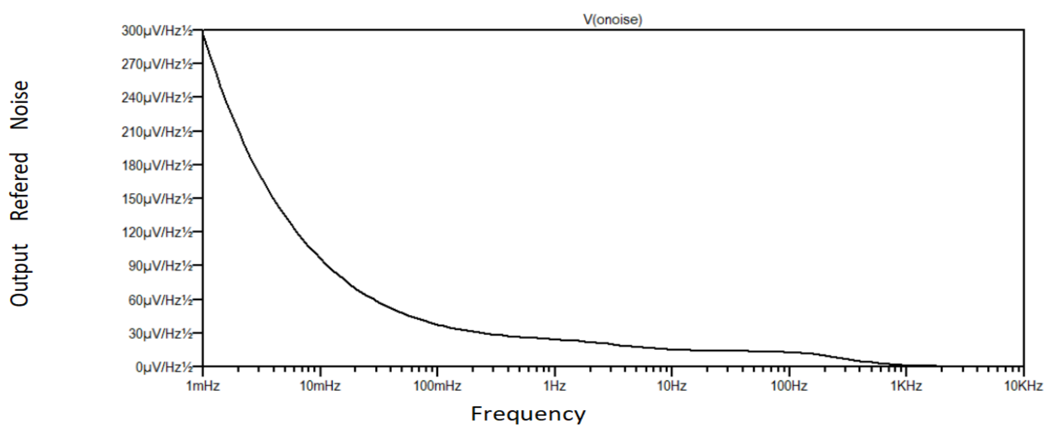

Figure 6. Noise analysis simulation.

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3.2. Discussion

Although wearable ECG testing devices are not as reliable as medical ECG testing devices, they provide a more convenient and fast way for people to observe their heart conditions at any time. Low power consumption and small size are important concerns among the devices that can be worn. The purpose of this project design is to create a circuit for a wearable ECG sensor that consumes minimal power and is small in size.

This project mainly simulates the designed sensor circuit based on LT-Spice software. Due to power consumption or volume, the design process should be minimized with the number of cases. So CMOS is used in circuits., because it can make the circuit have better impedance while also having a smaller size. When CMOS is in a subthreshold state, it consumes less power and has better linearity. So the use of CMOS can solve power consumption and volume problems. Zhong Zhang proposed the use of a capacitive coupling circuit to extract electrical signals. According to his experimental results, when the signal cutoff frequency is 1kHz, the circuit gain is 40dB, but the circuit power consumption is 48uW [10]. The project plays a relatively good role in terms of power consumption.

Next, the circuit is designed by adding a right-leg drive circuit to the traditional 3op-amp circuit. This improvement effectively solves the problem of common-mode noise in traditional 3-op-amp circuits and provides a more reliable and safe way to ground the human body. After the circuit design and parameter calculation, a series of functional analyses of the circuit are carried out. The first task is to perform an AC sweep of the circuit output between 1mHz and 1kHz to determine the gain size of the circuit on the constructed circuit. After that, it is necessary to detect the comprehensive output noise of the circuit from 1mHz to 10kHz and calculate the input reference noise of the circuit to determine the noise reduction ability of the overall circuit. The common-mode and differential-mode gains of the circuit are analyzed by calculation. At the same time, the noise effective factor and CMRR of the circuit are also calculated, to judge whether the comprehensive performance of the circuit is good.

Due to the limitations of experimental conditions, this project is not perfect enough. Whether it is from simulation to designing actual circuits, this project still needs a lot of experiments to improve. Because in the actual design process, there are a series of errors due to some temperature or circuit wiring and other reasons. In addition, this project has some prospects in the future. The resistance on the low-pass filter of this project takes up a certain volume for portable devices. It is not good enough, so This resistor should be replaced by a pseudo-resistor. At the same time in the future, the circuit should also add a detection system. When the device detects an abnormal ECG signal, the circuit should start alarming and alerting the user. When the device remains in an unhealthy state, the device initiates the call for ambulance function. The final point concerns power consumption. The current power consumption of the entire circuit is in line with the design standards. However, it is still high, mainly because there are more amplifiers throughout the design circuit. The circuit's power usage should be decreased, it is necessary to develop a strategy to decrease the number of amplifiers in the circuit in the future.

4. Conclusion

In this circuit, a new method is proposed in terms of circuit power consumption and circuit size. Through the simulation results of LT-Spice software, the performance indicators of the circuit can be obtained. According to the comparison, the performance of the circuit meets all the requirements of the practical application, especially in terms of size and power consumption. This is one of the important measures to measure the quality of wearable devices nowadays. This project allows wearable devices such as headphones or watches to perform ECG measurements. Help some people with heart disease to have their heart status checked at any time. It is more convenient and faster than some traditional medical devices that detect ECG. At the same time, the circuit needs some improvement in some aspects. As shown above, the resistance of the low-pass filter is replaced by a pseudo-resistor. Minimize the number of amplifiers in the entire circuit to decrease the power consumption of the entire circuit. This can greatly improve the ability to use wearable devices. The circuit added an alarm system to alert the user when

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the heart is in an abnormal state. This project can help many patients with heart diseases to detect their heart condition at any time.

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