Proceedings of the 3rd International Conference on Computing Innovation and Applied Physics
DOI: 10.54254/2753-8818/14/20240945

The influence of second-order effect on circuit design

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Abstract. The purpose of this paper is to deeply study and understand the influence of second-order effects (channel length modulation effect, bulk effect, subthreshold conductivity short channel effect) on the performance of electronic devices and circuits, and to propose effective methods and techniques to reduce their negative effects. The author will pay attention to the mechanism and characteristics of channel length modulation effect, bulk effect, subthreshold conductivity and short channel effect, and the key factors leading to their changes. Through theoretical analysis, process inversion and simulation, various effective suppression or compensation strategies are explored to improve the performance of electronic devices and circuits and enhance their reliability and stability. Through the in-depth study of the second-order effect, readers can better understand and solve the influence brought by the second-order effect.

Keywords: Channel Length Modulation Effect, Bulk Effect, Subthreshold Conductivity, Short Channel Effect.

1. Introduction

With the increasing demand for electronic devices with higher performance, greater function and lower power consumption in the market, the demand for transistors in the circuit is shrinking, while the demand for service frequency and life is greatly improved, so the second-order effect has become more significant for circuit design, which will lead to non-ideal behavior and performance degradation. The second-order effect of MOS transistor (metal oxide semiconductor field effect transistor) refers to the second harmonic and intermodulation caused by nonlinear characteristics in the working process of MOS transistor. In MOS transistor, when the input signal adjusts the conduction degree of the transistor through the gate control voltage, nonlinear distortion will appear in the output signal. Understanding and mitigating the second-order effect is very important for circuit designers to achieve the expected performance specifications. By studying the complexity of these impacts, we can gain valuable insights into their potential mechanisms and develop advanced design techniques to minimize their impacts. According to the development prospect of integrated circuit design industry in China, China is now facing the reality of both opportunities and challenges. The technology of integrated circuits has developed rapidly in recent years, but it still faces some technical problems [1]. The purpose of this paper is to study and solve the second-order effect in circuit design. Our goal is to explore the most common second-order effects encountered in modern electronic circuits and propose new methods for their analysis, modeling and mitigation. By fully understanding these influences and their influences, we can design more powerful and efficient circuits to meet the needs of the developing electronic industry.

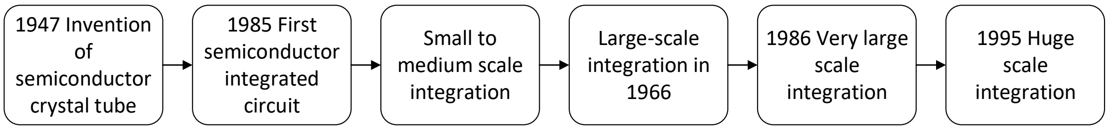

Figure 1. Development history.

Since the invention of semiconductor transistor [2] in 1947 with today's large-scale integrated circuits, the public demand has a higher demand for circuit integration, accuracy and low energy consumption, and the development of circuit design determines the development level of integrated circuits, which can be seen in figure 1,so it has an important impact on circuit design and manufacturing technology by reducing the influence of second-order effect on circuit design, thus improving circuit accuracy, performance, system reliability and reducing power consumption. In this regard, various technologies emerge one after another, such as gene expression programming proposed in 1992, which models and solves problems through gene expressions, automatically searches for solutions and generates high-quality programs, which simplifies our design process to some extent. At the same time, the further development and utilization of EDA software [3] based on the research and application of secondary development of EDA software is also convenient for us to better simulate and test the circuit model. Therefore, through appropriate design and optimization measures, the adverse effects on circuit performance can be reduced, nonlinear distortion can be reduced, and the linearity and signal quality of the system can be improved.

The purpose of this paper is to study and solve the second-order effect in circuit design. Our goal is to explore the most common second-order effects encountered in modern electronic circuits and propose new methods for their analysis, modeling and mitigation. By fully understanding these influences and their influences, we can design more powerful and efficient circuits to meet the needs of the developing electronic industry. In this paper, we have comprehensively studied the key second-order effects, including but not limited to channel length modulation effect, bulk effect and subthreshold conductive short channel effect. We deeply analyze their influence on circuit performance, discuss the existing mitigation technologies, and propose new methods to improve circuit design accuracy and stability. By searching data, a large number of simulations and experiments are carried out to prove the effectiveness of the experimental principle and method.

This paper is mainly divided into three parts, and the main ideas can be seen in figure 2: the first part is the introduction, which briefly introduces the development background and principle of the second-order effect. The second part is the text introduction, which mainly introduces the generation principle, derivation process, research and discussion of several second-order effects, the discussion of the influence of second-order effects on circuits and the corresponding solutions. The third part is a summary, including the research results and the prospect for the future.

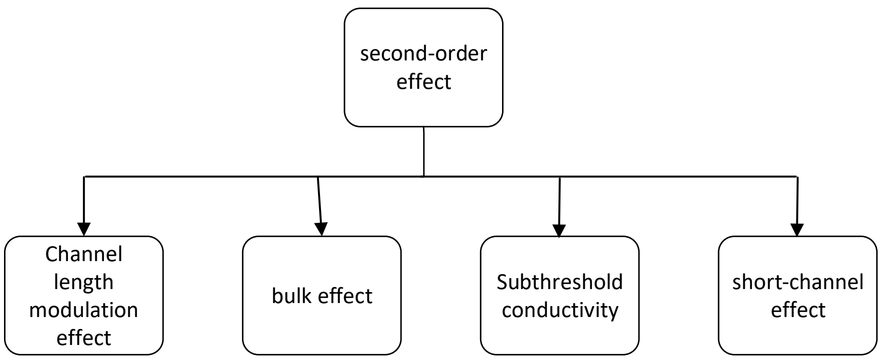

Figure 2. Article structure.

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2. Main body

2.1. Channel length modulation effect

2.1.1. Principle of production. The channel length modulation effect of MOSFET [4] means that with the change of gate voltage, the conductivity of the channel will also change. Especially in short channel length and high frequency applications, the channel length modulation effect will lead to nonlinear transmission characteristics and affect the gain, bandwidth and linearity of the circuit. The relationship between channel length, I_D and V_{DS} can be seen in Figure 3.

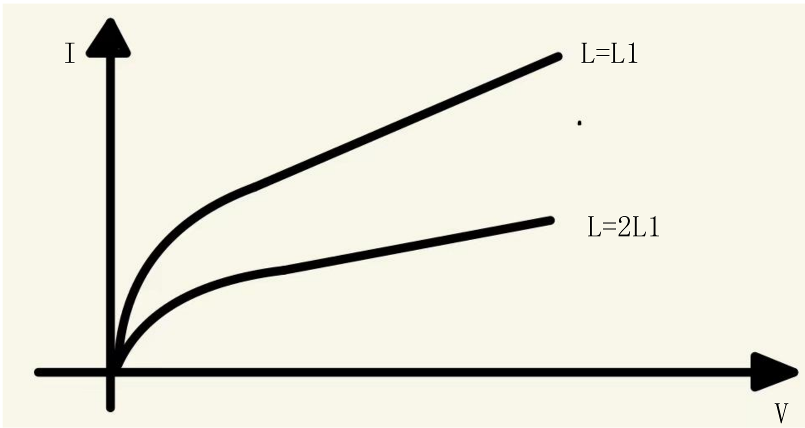

Figure 3. Influence of channel length on I_D and V_{DS}.

2.1.2. Impact on circuit design. First, increase the nonlinear relationship between current and voltage: the channel length modulation effect leads to the nonlinear dependence of drain-source current on channel length.

Second, affect the gain of the amplifier: The channel length modulation effect will affect the output characteristics of MOSFET. When the transistor is used as an amplifier, the nonlinear channel length modulation effect will lead to the change of gain.

Third, affect the switching speed: The channel length modulation effect will also affect the switching speed of the transistor. When the channel length is shortened, the capacitance of the transistor (such as effective output capacitance [5], input capacitance, etc.) will also decrease, resulting in faster switching speed.

Forth, power consumption and temperature characteristics: the channel length modulation effect will lead to the increase of drain-source current, which will increase the power consumption of the transistor in the saturation region. In addition, the channel length modulation effect may also affect the temperature characteristics of the transistor, such as the sensitivity of temperature to conduction characteristics.

2.1.3. Solution. First, optimize the device size and structure: By properly selecting the transistor size and structure parameters, the influence of channel length modulation effect can be reduced. For example, increasing the channel width (w) can reduce the channel resistance, thus reducing the influence of channel length modulation effect on transistor characteristics.

Second, using special materials and processes: Using some special materials and processes can reduce the channel length modulation effect. For example, introducing materials with high dielectric constant, such as high k gate oxide, can reduce the channel capacitance, thus reducing the piezoelectric effect. In addition, the channel length modulation effect can also be reduced by adopting some advanced process technologies, such as multi-pillar package (FinFET) and floating gate.

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Third, design optimization and compensation techniques: In circuit design, some optimization and compensation techniques can be used to reduce the influence of channel length modulation effect. For example, an active bias circuit is used to automatically adjust the operating point of the transistor to offset the influence caused by the channel length modulation effect. In addition, using special current source and current mirror circuit can also improve the influence of channel length modulation effect on circuit performance.

Forth, accurate modeling and simulation: In the process of circuit design, it is very important to accurately establish and simulate the channel length modulation effect. Using accurate models and simulation tools, we can better understand, predict and optimize the influence of channel length modulation effect on circuit performance. This is helpful for designers to optimize and adjust effectively in the early stage.

2.2. Body effect

2.2.1. Principle of production. Body effect refers to the formation of a depletion layer in the Channel-Substrate Junction due to the action of the gate electric field in a MOSFET, thus affecting the conductivity of the channel region. $V_B \neq V_S$ With the increase of V_{SB}, the threshold voltage VTH will also increase. The effect of the change of body potential on the threshold voltage is called body effect, also called back gate effect. For example, in a source follower circuit which can be seen in figure 4, if there is no volume effect, V_{OUT} increases synchronously with the increase of V_{IN}. However, due to the existence of volume effect, V_{OUT} will also increase with the increase of V_{IN}, but the increase of V_{OUT} will increase V_{IN}, and finally the growth rate of V_{OUT} will slow down.

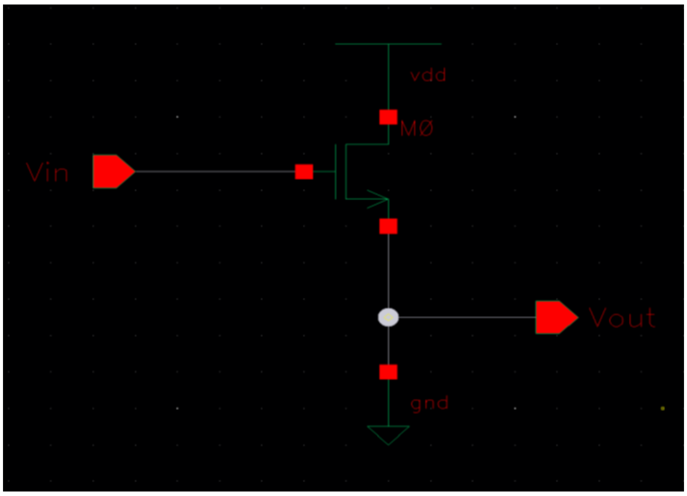

Figure 4. Circuit diagram of the source follower.

2.2.2. Derivation process. When $V_B<V_S$, with the decrease of V_B, holes are attracted to the substrate electrode, the depletion layer is widened, and the charge Q_{dep} in the depletion region increases, resulting in an increase in V_{TH}.

$$V_{TH} = \varphi_{MS} + 2\varphi_F + \frac{Q_{dep}}{C_{ox}} \tag{1}$$

Body effect coefficient γ

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{|2\varphi_F + V_{SB}|} - \sqrt{|2\varphi_r|}\right) \tag{2}$$

Its typical value is

$$\gamma \sim 0.3 - 0.4V^{1/2} \tag{3}$$

Designers determine γ by weighing the substrate concentration Nsub and the gate oxygen capacitance C_{ox}.

2.2.3. Impact on circuit design. First, influence of threshold voltage: When the gate voltage under forward bias exceeds the threshold voltage, the MOS transistor turns on and conducts current. Therefore, the threshold voltage of the gate will directly affect the operating characteristics of the circuit and the voltage range above the threshold voltage.

Second, channel length modulation effect: The channel length modulation effect of MOS transistor will cause nonlinear change of current. Channel length modulation effect refers to the change of channel resistance or conduction current due to the change of channel voltage under different gate voltages. This will affect the gain, power consumption, speed and other performance indicators of the circuit.

Third, power supply drain broadening effect: When the MOS transistor is turned on and the drainoltage is high, the current distribution will expand in the drain region with the electric field, which will lead to the increase of current and the distortion of the circuit.

Forth, power consumption effect: MOS tube effect will lead to leakage current in non-conductive state, which is caused by the charge of the emptying layer. These leakage currents will increase the static power consumption of the circuit, especially in large-scale integrated circuits, which may significantly affect the power consumption.

2.2.4. Solutions. First, optimization of process parameters: Select appropriate process parameters, such as substrate doping concentration and thickness, to control the influence of bulk effect. The optimization of process parameters can reduce the non-uniformity of current transmission and electric field distribution in the substrate, thus reducing the negative influence of bulk effect.

Second, introduce substrate bias: use Body Biasing technology to adjust the voltage relationship between substrate and source/drain. By adjusting the substrate bias voltage, the threshold voltage and intensity of the transistor can be changed, and the influence of body effect can be reduced. Substrate bias can improve the stability and performance of transistors.

Third, design appropriate power supply/pin connection: Design the connection mode of power supply and pin reasonably to avoid loss and noise. Good connection and layout can reduce the problems of power feedback, current drift and voltage drop, thus reducing the influence of body effect.

Forth, optimization of circuit: By optimizing the circuit structure and layout, the distance and interference between devices are reduced. Reasonable circuit structure can reduce the mutual influence and coupling effect caused by body effect [6],and improve the stability and anti-interference ability of the circuit.

Fifth, use suppression technology: Use specific suppression circuits and technologies to reduce the influence of body effect. For example, the suppression circuit is introduced to compensate the threshold voltage drift caused by bulk effect, or the optimization of process characteristics and materials is used to reduce the influence of bulk effect.

2.3. Subthreshold conductivity

2.3.1. Principle of production. Definition: V_{GS}, which makes the silicon surface in the intrinsic state, is called the intrinsic voltage, and is recorded as V_i. When $V_{GS} = V_i$, the surface potential $\phi_S = \phi_{FB}$, the energy band bending amount is qφr, and the surface is in an intrinsic state.

When $V_i < V_{GS} < V_T$, $\phi_{FB} < \phi_S < 2\phi_{FB}$,the surface is in a weak inversion state, and the minority carrier (electron) concentration in the inversion layer is between the intrinsic carrier concentration and the substrate equilibrium multi-carrier concentration. At this time, the drain-source current is called subthreshold current.

2.3.2. Impact on Circuit Design. First, drain current and power consumption: The conductivity of the subthreshold region makes a small amount of current pass in the subthreshold region, which will lead to additional drain current in the circuit. Subthreshold current will increase the power consumption of the circuit, especially when there are a large number of MOSFET. In the circuit design, it is necessary to evaluate and control the subthreshold current reasonably to ensure that the power consumption of the design meets the requirements.

Second, temperature effect: subthreshold conductivity is closely related to temperature. The subthreshold current increases with the increase of temperature, which is due to the thermal excitation of electrons and the temperature dependence of energy tunneling effect. In high temperature environment, the increase of subthreshold current will significantly affect the performance and stability of the circuit. Therefore, the temperature effect of subthreshold current should be considered in circuit design in high temperature environment, and corresponding measures should be taken for thermal management and compensation.

Third, bias circuit design: Because of the existence of subthreshold conductivity, the influence of subthreshold current should be considered in bias circuit design. Subthreshold current will lead to the change of bias point of bias circuit, which will affect the working state and performance of the circuit. In the design of bias circuit, it is necessary to choose the structure and parameters of the circuit reasonably to realize stable bias and offset the influence of subthreshold current on the circuit performance.

Forth, timing and clock design: The existence of subthreshold current will increase the response time of the circuit in subthreshold region, which has certain challenges for timing and clock design. In the design of high performance clock and timing, it is necessary to consider the delay effect of subthreshold current and take corresponding measures to ensure the accurate transmission of signals and the stability of timing.

2.3.3. Solutions. First, optimize the size and process of MOSFET: By optimizing the size and process parameters of MOSFET, the influence of subthreshold conductivity can be adjusted. For example, reducing the length of MOSFET and increasing the thickness of gate oxide can increase the gate control effect and reduce the conductivity of subthreshold region.

Second, increasing the threshold voltage: Increasing the threshold voltage of MOSFET can effectively reduce the sub-threshold conductivity. By adjusting the process parameters such as substrate doping concentration and gate material, the threshold voltage can be adjusted.

Third, adopting proper bias circuit: In the circuit design, the influence of subthreshold conductivity is offset by designing proper bias circuit. For example, the compensation and stable bias of subthreshold current can be realized by using drain negative feedback or reference current source.

Forth, strengthen thermal management: The sub-threshold conductivity is related to temperature, so strengthening the thermal management of the circuit can reduce the influence of sub-threshold conductivity on the circuit. Using radiator and temperature sensor to keep the circuit working in a suitable temperature range can reduce the influence of subthreshold current.

Fifth, optimizing timing and clock design: Considering the delay effect of subthreshold current, the influence of subthreshold conductivity on the circuit can be reduced by optimizing timing and clock design. For example, reasonably set the signal delay and timing constraints to ensure that the response time of the circuit in the subthreshold region meets the requirements.

2.4. Short channel effect

2.4.1. Principle of production. Short Channel Effect means that when the channel length of a metal oxide semiconductor field effect transistor (MOSFET) is reduced to a small size range, the electric field distribution and control characteristics between the channel region and the source and drain change, which leads to non-ideal effects of device characteristics.

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2.4.2. Impact on Circuit Design. First, threshold voltage change: Short channel effect will cause the threshold voltage of MOSFET to change. The change of threshold voltage will lead to the deviation of the on and off characteristics of equipment, which will affect the working state and performance of the circuit.

Second, leakage current increase: the electric field and sidewall effect caused by short channel effect will lead to the increase of leakage current. High leakage current will generate additional power consumption and lead to the increase of circuit power consumption.

Third, equipment aging: Due to the high electric field and local thermal effect caused by short channel effect, more carrier injection, heat generation [7] and dielectric aging will occur in the equipment. These factors will reduce the life and reliability of the circuit.

Forth, speed reduction: Short channel effect will reduce the speed of equipment. Due to the uneven electric field caused by short channel effect, the increase of channel resistance and the high-speed saturation of carriers, the signal transmission speed will slow down, limiting the response time and working frequency of the circuit.

Fifth, power supply jitter: the decrease of channel length will increase the source-drain resistance, leading to greater power supply jitter and power supply noise. This may affect the stability and anti-interference ability of the circuit.

2.4.3. Solution. First, optimize the size and process parameters of MOSFET, and reducing the influence of short channel effect by using a non-planar transistor channel structure [8], increasing the thickness of gate oxide layer and carrying out heat treatment [9].

Second, adopt optimized bias circuit design, and offset the influence of short channel effect on circuit performance by negative feedback or reference current source.

Third, appropriate source and drain structures and materials are adopted to reduce the diffusion effect of source and drain current.

Forth, optimize the design of power supply and signal line to reduce power supply jitter and noise.

Fifth, temperature compensation technology [10]: Because the short channel effect will have a greater impact on the temperature change, the use of temperature compensation technology can reduce its impact on the transistor performance. For instance, the thermal feedback mechanism can realize the adaptive adjustment to the temperature change and improve the stability and consistency of the transistor.

3. Conclusion

The channel length modulation effect leads to the nonlinear relationship between the output current and the input voltage of MOS transistor. When the gate-source voltage increases, the channel resistance decreases due to the channel length modulation effect, which leads to the increase of output current. On the contrary, when the gate-source voltage decreases, the channel resistance increases due to the channel length modulation effect, which leads to the decrease of the output current.

The existence of MOS tube body effect will cause the channel current to change with the change of backing voltage. When the backing voltage increases, the PN junction in the backing region will become shallower, forming a lower depletion region, thus reducing the capacitance effect of the depletion region and leading to an increase in channel current; On the contrary, when the backing voltage decreases, the PN junction in the backing region will become deeper, forming a larger depletion region, increasing the capacitance effect of the depletion region, resulting in a decrease in channel current.

The subthreshold current is related to temperature, substrate doping concentration, gate length and other factors. In the actual circuit design, it is necessary to control and compensate the sub-threshold conductivity reasonably to ensure that MOSFET can work in the expected way and avoid power consumption and performance problems in the circuit. However, the short channel effect makes the classical square law transmission characteristics of MOS transistors more linear in saturation region or amplification region.

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With the continuous improvement of technology, integrated circuits in the future will be able to integrate more functions and modules, with higher working frequency and lower power consumption, higher system performance and more diversified applications. At the same time, with the development of new materials and technologies, the design of integrated circuits will continue to innovate to meet the needs of the public and face challenges.

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