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Advantages of FINFET over traditional CMOS: Reasons and implications

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Abstract. In the relentless march of technological advancement, the semiconductor industry remains at the forefront of innovation. Among the myriad breakthroughs, FinFET technology stands out as a recent focal point in research. Serving as an avant-garde semiconductor manufacturing process, FinFET plays a pivotal role in enhancing chip performance, diminishing power consumption, and minimizing component size. At its core, FinFET is a distinct type of field-effect transistor (FET) that utilizes a thin silicon "fin" as the conducting channel. This structure has revolutionized the way transistors are designed, offering remarkable control over the current flow through the channel. This control is achieved by wrapping a gate material around the three visible sides of the fin, which provides superior switching behavior and leakage reduction. Beyond its foundational principles, FinFET's inherent characteristics offer numerous advantages. For instance, the technology paves the way for more densely packed transistors, enabling more powerful yet compact integrated circuits. Moreover, its innovative design leads to more energy-efficient chips, which are crucial for today's demanding computing and electronic environments.

Keywords: FINFET, CMOS, Size, Power Consumption, Integrated Circuit.

1. Introduction

The Fin Field-Effect Transistor, commonly known as FinFET, derives its name from the unique fin-like shape of the transistor. Unlike the traditional two-dimensional planar structures, FinFET boasts a three-dimensional architecture, offering enhanced efficiency coupled with reduced energy consumption. This three-dimensional design not only allows for a more compact size but also delivers quicker response times and diminished power usage compared to conventional CMOS devices.

One of the most noteworthy attributes of the FinFET design is its capability to improve the control of electrical circuits, significantly reducing the leakage current. As a result, it is possible to achieve shorter transistor gate lengths. This reduction in leakage and enhanced control offers a myriad of benefits, which become evident when considering the technological advancements and power constraints of today's devices [1]. Given its advantages, FinFET technology is aptly positioned for fabricating integrated circuits used in various domains. Whether it's high-performance computing, which demands rapid processing speeds and efficient energy utilization, or mobile communications that require reliable and power-efficient chips, FinFET stands out as a prime choice. Moreover, in the burgeoning world of the Internet of Things (IoT), where millions of devices communicate and operate on constrained energy

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sources, the efficiency and reduced power consumption offered by FinFET technology becomes invaluable. In sum, the FinFET technology's three-dimensional structure provides a strategic edge in contemporary circuit design, paving the way for the next generation of electronics in an increasingly connected world.

2. Advantages of FINFET

2.1. Lower power consumption

Improvements in the energy efficiency of ICs have largely been achieved through voltage reduction. Over the years, the consistent decrease in the feature size of CMOS technology has driven noteworthy enhancements in circuit speed and average cost [2]. Yet, as we attempt to shrink traditional planar CMOS transistors beyond 22nm, challenges arise due to the constraints of basic materials and process technologies. Notably, how can the industry mitigate the short-channel effect and minimize leakage current. Short channel effects arise when the length of the conducting channel of a metal oxide semiconductor FET diminishes to the scale of tens or even a few nanometers [3]. As integrated circuit sizes are scaled down, so is the size of the transistor channels. Initially, electron flow from the source to the drain is managed by the gate voltage. However, a reduced gate length diminishes the contact area between the gate and the drain. Consequently, the influence of the gate on the drain amplifies, diminishing gate-to-drain control and leading to a weakened gate voltage containment [4]. These short channel effects encompass a variety of issues including decreasing threshold voltage with reduced channel length, barrier reduction due to depletion, surface scattering of carriers, velocity saturation, ionization, and thermoelectronic effects. Such effects can escalate energy consumption and can even render the device nonfunctional [5].

A salient difference between the FinFET and the traditional MOSFET is the FinFET's distinctive structure: its channel exhibits tall, thin fins erected on an insulating substrate, with its source and drain at either end. Importantly, the three gates of the FinFET are proximate to its sidewalls and top. This structural enhancement wraps the gate around the channel, fortifying the channel's control via the gate. Such a configuration mitigates the short channel effects, enhances circuit control, curtails current leakage, and allows the use of a longer gate in the transistor. Furthermore, the FinFET does not require heavy doping of its channel, minimizing the interference of impurity ions and fostering improved carrier mobility within the channel. As for carriers, they signify the cumulative movement rate of electrons and holes in a semiconductor [6]. Carrier mobility depicts the average drift speed of carriers (both electrons and holes) under the influence of a unit electric field. Higher mobility translates to quicker carrier movement and vice versa. It's noteworthy that different carrier types within the same semiconductor material exhibit varied mobilities, with electron mobility typically surpassing hole mobility. Concurrently, FinFET devices present an advantage in reducing gate leakage current. Gate leakage current refers to the internal current within a MOS tube in the absence of an externally applied voltage. This current primarily emerges due to the thermally stimulated movement of electrons in semiconductor materials and the semiconductor's surface state. The magnitude of the leakage current is influenced by factors such as material quality, surface state density, and the manufacturing process. Its presence is detrimental for several reasons: Firstly, it directly adds to the power dissipation, elevating the static power consumption of the circuit [7]. Secondly, the heat generated from this power loss can raise the circuit temperature, potentially compromising the circuit's stability and reliability. Thanks to their capacity to quash the short-channel effect and augment gate controllability, FinFET devices allow the employment of thicker gate oxides compared to planar devices, effectively curtailing gate leakage current.

2.2. Higher speed

he subthreshold swing S quantifies the transition speed between the on and off states of a transistor. Ideally, this switch should be binary. This means that, when the voltage exceeds Vt, it should reach saturation current, and when it's below Vt, it should return to zero immediately. Typically, any current

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below the threshold isn't desirable. Rapid movement through the threshold area is preferable, ensuring prompt device usability, which in turn minimizes unwanted power wastage and heat production. S represents the amount of gate voltage change required to change the source leakage current by a factor of ten, and a smaller S means a faster turn-off rate [8]. The unit of S is usually mV/dec, which is the amount of change in gate voltage when the drain current changes by an order of magnitude (10 times). Currently, the limit value of S at room temperature is about 60mV/dec, and it is difficult to reduce it as the size of the device decreases. In FinFET, as the thickness of the silicon Fin decreases, the lower slope of the threshold also decreases and approaches the ideal value of 60mV/dec. This is due to the fact that as the surrounding thickness decreases, the gate control ability of the channel gradually increases and the blocking effect of the short channel also increases.

2.3. Smaller size

As technology continues to advance, the size of transistors is gradually reduced, which brings many significant advantages.

These mainly include the optimization of power consumption, speed and reliability. Smaller transistors mean lower power consumption under the same conditions. This helps improve the battery life of your device, especially in portable devices [9].

At the same time, reducing the size of the transistor allows for faster propagation of the signal in the circuit. Because the switching speed of the transistors limits the speed of the CPU. According to the principle of capacitor charging, the switching speed and capacity depend on the size of the capacitance. The larger the capacitor, the longer the charging time and the slower the startup. Therefore, need to reduce the capacity to increase the operation speed. This means that the device can process more data at the same time, improving overall performance.

$$C = \frac{\varepsilon \cdot A}{d}$$

C is the capacitance, which is the dielectric constant A is the plate area ε is the dielectric constant d is the thickness of the dielectric layer. From this formula, it can be seen that reducing capacitance can be achieved in three ways: increasing the thickness of the dielectric layer, changing the dielectric constant, and reducing the area. However, too large a dielectric layer thickness may result in insufficient electric field in the channel and thus lead to conductivity failure; Changing the dielectric constant requires replacing the dielectric material, and the selection of dielectric materials for long-term use is very limited. Thus, the only useful way is to reduce the area, which means reducing the length and width of the channel. As a result, transistors followed this strategy and kept shrinking. In addition, the reduction of transistor size can reduce the probability of failure due to thermal effects and electromagnetic interference (EMI), etc., thereby improving the reliability of the device. After solving the problems caused by the short channel effect and leakage current, FINFET technology further reduces the size of the transistor to less than 22 nanometers.

2.4. Higher level of integration

The three-dimensional structure of FinFETs allows it to achieve higher transistor densities on the same chip area than conventional planar FETs [10]. This means that FinFET can provide higher performance at the same manufacturing cost. At the same time, FINFETs can have more transistors in the same area, which enhances the computing power of FINFETS.

3. Challenges and prospects

With the continuous shrinking of the chip manufacturing process, FINFET process devices struggle to cope with the size of less than 5 nanometers, and the leakage current and short channel effect have reappeared. And with the miniaturization process, if three fins can be placed on a FinFET transistor, now only one can be placed, so the fins need to be enlarged. However, as the fins become taller and taller, it is difficult to maintain an upright position under internal voltage after a certain height, and it is difficult

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to form a FinFET structure. The most likely process to replace FINFET is GAAFET. GAAFET is equivalent to an improved version of 3D FinFET, the structure of the transistor within this technology has changed again, the drain and gate are not like fins anymore, but have become something look like small stick that pass vertically through the gate, so that the gate can be wrapped from all sides of the source and discharged.

It looks like the original source electrode drain semiconductor was a fin and now the gate has become a fin. So GAAFET and 3D FinFET have many similarities in implementation principles and ideas. Since the source semiconductor and the drain semiconductor are separated by three to four contact areas and are also divided into several four contact areas, the gate current control is further improved. In addition, this GAA design can also solve the FinFET fin pitch reduction problem and largely solve problems caused by gate pitch reduction such as capacitive effects. These properties allow a process lower than FINFET to be manufactured.

4. Conclusion

As an improvement of the traditional CMOS process, FINFET changes the size of contact surface between the channel and the gate from one to three, increases the contact area of the channel and gate under the same size, thereby enhancing the voltage control ability of the channel, and solving the increase in energy consumption and reliability reduction caused by the short channel effect. The chip manufacturing process continues to extend downward from 22 nanometers. At the same time, due to the reduced size, FINFETs also have lower latency due to smaller capacitance, and more transistors in the same area. These factors allow FINFETs to have lower power consumption, faster speeds, and larger circuit sizes than traditional CMOS devices. However, at the same time, when the chip process is reduced to less than 5 nanometers, the FINFET will also produce a short channel effect due to the weakening of the ability to control the channel, and it will also be difficult to support because the fins are too high. Therefore, the GAAFET wrapped from four sides of the gate also came into being.

With the development of FINFET, GAAFET and more technologies, the new energy of chips will become more and more powerful, and the problems that can be solved are becoming more and more diverse. With the development of technologies such as artificial intelligence that require a lot of computing power, climate change that was previously difficult to predict may be accurately predicted, computing tasks that previously required a lot of manpower may be easily solved by artificial intelligence, and experiments that were previously difficult to carry out will be easily simulated by computers. At the same time, the increasing power of artificial intelligence will always remind humans what advantages humans have left in the face of these powerful machines.

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